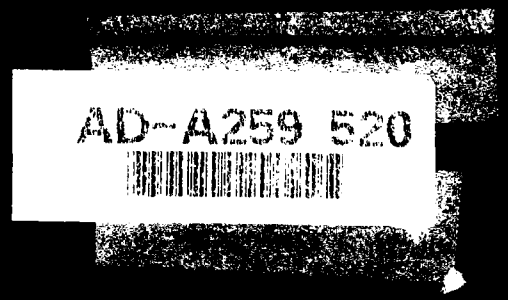

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SECTION I

FINAL REPORT

Applicability of Superconducting Interconnection Technology for High Speed ICs and Systems

Contract N00014-90-C-0217
BAA 90-06

Final Report

1.0 Introduction and Summary

This report represents the Final Report on Contract N00014-90-C-0217, BAA 90-06, "Applicability of Superconducting Interconnection Technology for High Speed ICs and Systems". Additionally, this volume includes the previous four quarterly reports issued as part of this effort.

The extremely low-loss characteristics of HTSC interconnect renders it an attractive candidate for high density-high performance digital circuitry. The purpose of this program was to investigate these properties in detail, and to determine the characteristics of systems that can best exploit these properties. To this end a study was undertaken to more fully characterize the limitations of conventional interconnect, in particular in the context of source-terminated CMOS devices, a technology well-adapted to cryogenic applications. Thermal and mechanical considerations of HTSC-MCM technology were explored as well as part of this effort. Applying Rent's Rule to system connection requirements, it was determined that HTSC interconnects can significantly reduce the required levels of wiring and/or increase the packing density of conventionally partitioned IC's on an MCM. This advantage is amplified if IC's are first optimized for MCM application (eg. using larger numbers of area-I/O pads at the chip levels). Commercial applications of the technology were likewise explored, and it is believed that the development of conventional cryogenic-MCM optimization technology could prove to be a useful first step in the development of an appropriate HTSC-MCM infra-structure. In conclusion, it is felt that HTSC-MCM technology has the potential to become a high-payoff commercially viable future technology for high performance digital packaging.

1.1. Background

1.1.1. High Performance Electronic Packaging Using Multi-Chip Modules with Superconducting Interconnects

While the focus of this program is on the applicability of superconducting interconnection technology for high speed systems, a major aspect of the effort is on understanding the limitations of conventional interconnect materials in advanced packaging applications. Multi-chip module (MCM) packaging of digital electronic systems not only allows for reductions in size and weight by using bare integrated circuit (IC) die (instead of individually packaged circuits) mounted with high density, but allows for higher system operating speeds as well. This higher performance is made possible because the distances between the various IC chips are reduced, which correspondingly reduces the time delay (propagation delay) experienced by signals going from one part of the system to another (the velocity of such signals being limited by the speed of light). Since the clock period (or time required to do an elementary operation) must exceed the sum of this signal propagation delay plus the time it actually takes the IC chips to perform their logic functions, the system performance can only be increased if both the logic and interconnect delays are reduced. In recent years, improvements in semiconductor technology have sharply increased IC speeds, but it has become increasingly difficult to achieve the full measure of this benefit in higher system speeds because of packaging limitations.

The highest density, and hence shortest interconnect delays, are achieved when an MCM substrate, large enough to hold all of the chips required, is essentially "tiled" with IC die, mounted as closely together as the bonding technology allows. This type of large, very high density, "system on an MCM" module is illustrated in Figure 1.1. with such maximal density MCM packaging, a single 6" MCM substrate might hold 500 or more VLSI chips, allowing a complete very high performance system to be placed on a single MCM. Unfortunately, it is extremely difficult to fabricate such an

Maximal-Density HTSC MCM "System on a Substrate"

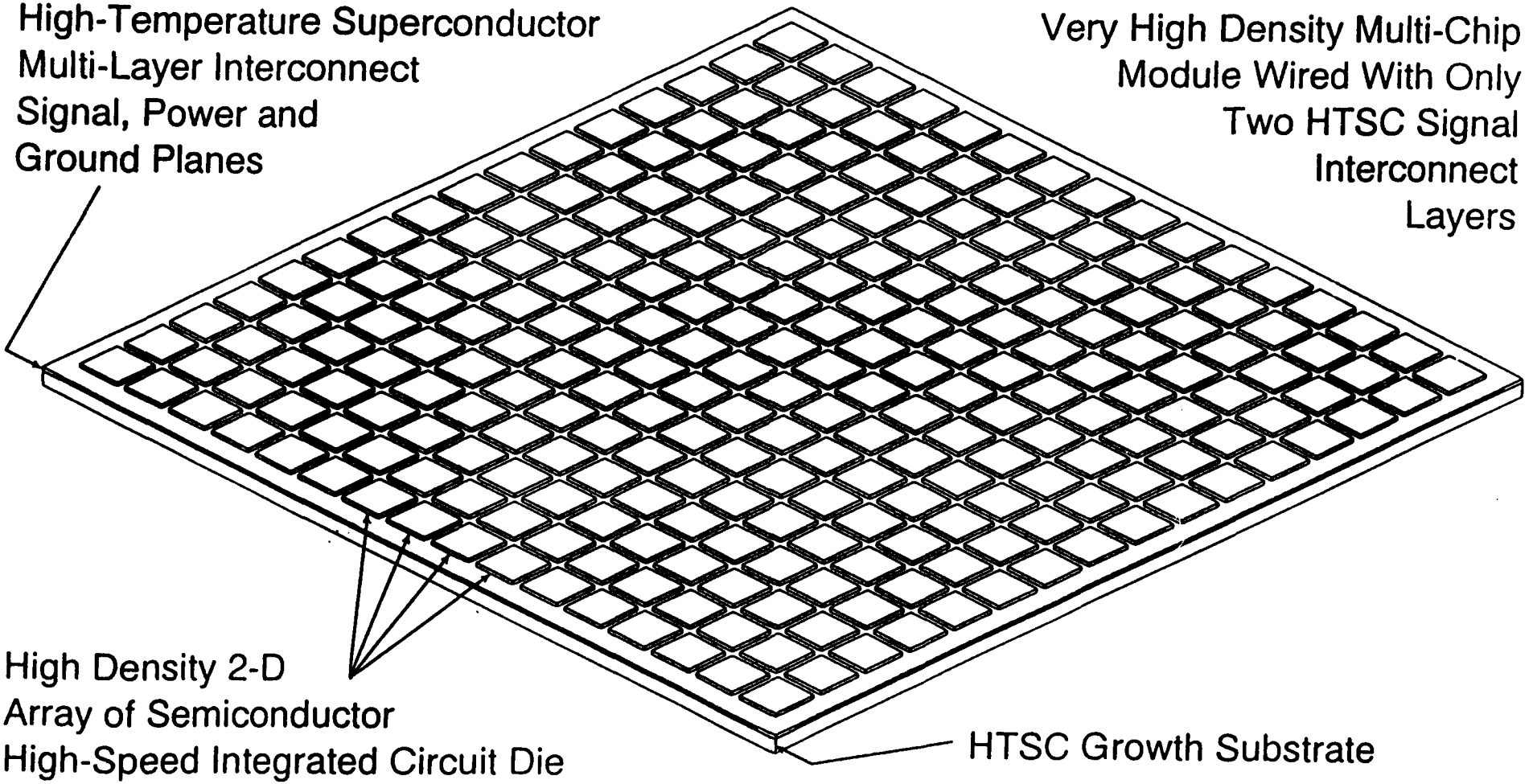


Figure 1.1

MCM using conventional metal (eg., copper) interconnects because the resistivity of normal metals are too high. For this 6" MCM example, over 100,000 signal interconnect wires would be needed to make the connections between the VLSI chips, requiring a total wire length of nearly two miles on the MCM! Actually, the lithography used in IC fabrication is capable of producing this much wire with only two layers of 1.5μm wide signal lines (on a 6μm pitch), but with normal metal lines, their resistance would be hopelessly too high (4600Ω for a 12" copper line, whereas it should be 50Ω or less for proper signal propagation). With normal metals, the only way to keep the line resistance low enough is to make the wires bigger in area, which reduces the density of the wires in each signal interconnect layer, necessitating the use of very large (impractically large from a fabrication standpoint) number of metal interconnect layers. For example, for the 6" MCM case discussed, over 60 copper signal wire layers would be required.

High temperature superconductors (HTSCs) offer an exciting solution to this high density MCM dilemma. These materials, when cooled to cryogenic temperatures of the order of 77°K, have essentially zero resistivity, and hence could in principle be used to wire such maximal density MCMs with only two signal interconnect layers. Not only would this make fabrication of such large "system on a substrate" MCMs with their very short interconnect signal propagation delays practical, but there would be a matching reduction of the logic delay as well. Because the velocities and mobilities of the electrons or holes in the semiconductor devices from which the ICs are built are greatly increase at low temperatures, typically the logic delays are reduced by a factor of about 2.5 when the chips are operated at the same temperatures as would be used for HTSC interconnections.

Implementation of a digital electronic system in an HTSC MCM packaging approach, through the balanced reduction of logic delay (from low temperature IC operation) and signal interconnect propagation delay (from maximal density packaging), offers a major increase in system performance (eg., 2.5 time faster) over normal systems using the same type of ICs. In other words, if a computer could run

at an 100MHz clock rate normally, then 250MHz should be achievable using HTSC MCM packaging, which would greatly increase its value (eg., if it were worth $1M with conventional packaging, it would be worth about $2.5M in the HTSC MCM version). Of course, in many military applications the fact that the size and wight have been dramatically reduced (to a single 6" x 6" substrate) is of crucial importance, over and above the fact that one faster processor can do the work of 2 to 4 normal ones (which further save size, weight, cost and power).

While the advantages of the use of HTSC interconnects in digital MCMs are obvious and impelling, substantial research and technology development effort will be required to achieve this result. The signal current densities in the fine (eg., W = 1.5μm or 2μm) superconducting signal lines are achievable at present only with high quality thin film HTSC materials. These are generally grown on crystalline substrates in a single flat layer, whereas the MCM application requires the growth of several patterned layers with thick layers of reasonably low dielectric constant insulators (crystalline or amorphous) in between them, as illustrated in Figure 1.2. In addition to these basic HTSC materials growth issues, it will be necessary to develop a practical HTSC MCM fabrication process for making HTSC MCM structures like that shown in Figure 1.2, including not only growing and patterning the HTSC signal and power and ground planes separated by the appropriate dielectric layers, but handling the interlayer via connections, die attach and lead bonding, supply bypassing, I/O connection, etc. problems as well. In addition, there needs to be associated with the technology development effort a strong electronic systems presence to provide focus to insure that the HTSC MCM technology developed will be appropriate for realistic digital systems applications.

The needs of this HTSC MCM technology development effort extend from basic HTSC materials research through fabrication process development to the creation of a business base capable of commercially supplying such a technology for a wide variety of high performance digital systems applications, both military and commercial. This will, of necessity, require a team effort to accomplish these ends,

Completed Simple HTSC MCM Cross-Section

(After IC Die Attach and Wirebonding Operations Completed)

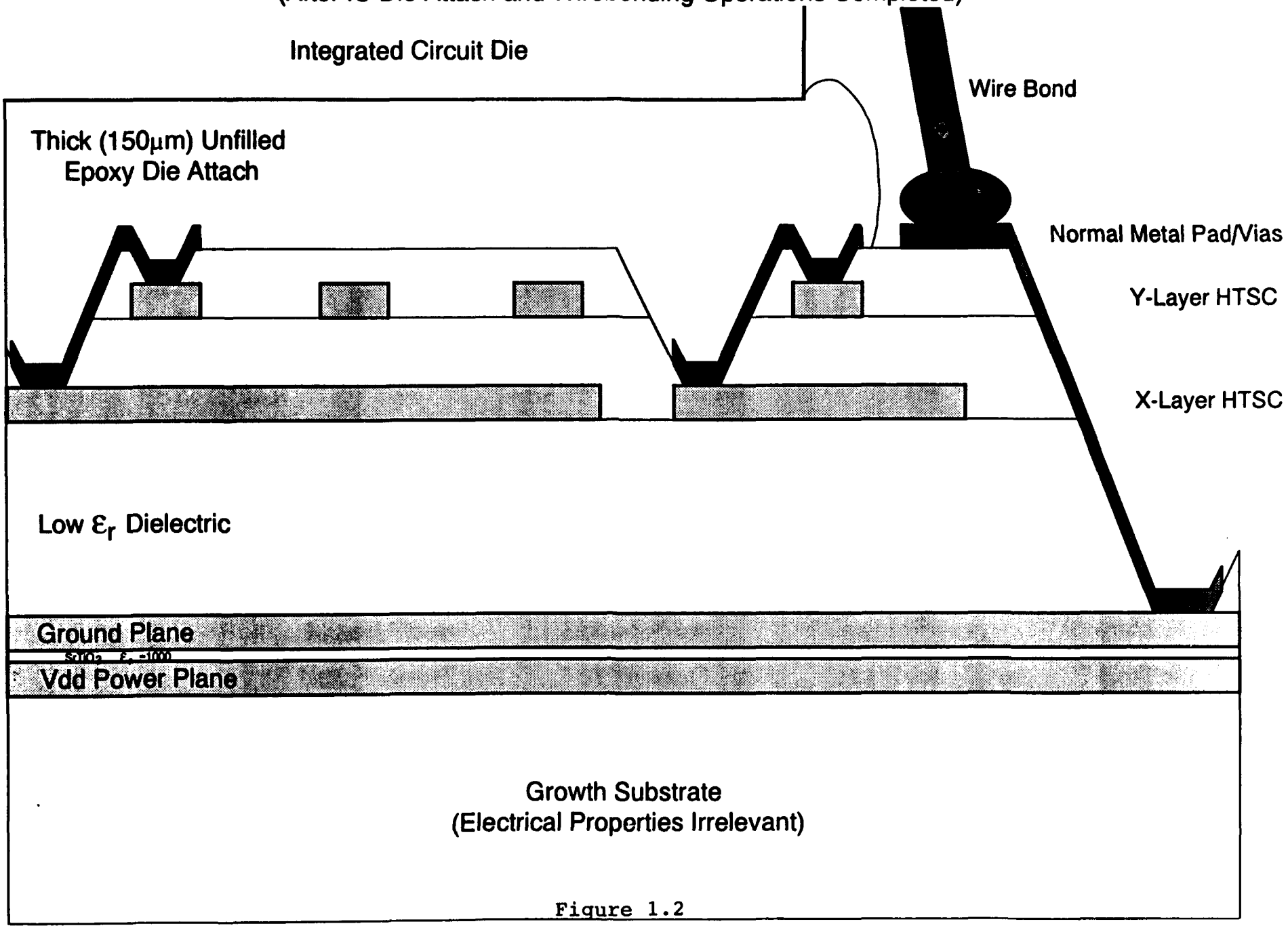


Figure 1.2

with involvement of universities (for basic HTSC materials research), merchant HTSC companies (within which to develop the HTSC MCM technology to insure it becomes commercially available to all US companies), and companies capable of furnishing required supporting technologies (eg., cryogenic coolers and packaging, ICs, testing, CAE tools, etc.), plus an electronic systems house to maintain the proper applications focus to the effort.

The payoff from such an HTSC MCM technology development effort should be enormous. Not only would such commercial digital electronics systems as computers (eg., supercomputers, mainframes, mini-supercomputers and super-minicomputers), communications systems and specialized signal processors such as pattern recognition or medical imaging systems be potential applications, but a wide variety of military signal processing (eg., RADAR, ELINT, ECM, "smart weapons", etc.), communications and other military system applications could greatly benefit from this exciting technology as well. In addition to MCM substrate applications, the same HTSC technology to be developed for HTSC MCMs could be applied to many other applications as well. For example, this HTSC MCM technology could be utilized to implement an HTSC backplane which, in only a 6" width, could achieve a 2.5 Terabits/second raw data transfer rate at clock rate of only 100MHz, or up to 250 Terabits/second if the ICs were fast enough to handle a 10GHz clock rate (that rate would be no problem for the fineline HTSC interconnects). This is only one of many other possible applications for this exciting technology.

1.2. Commecial Applications

We began this program knowing that if HTSC-MCM technology could be developed and the benefits of lower temperature operations are realized, the MCM industry would still encounter difficulties having this technology accepted by the high volume commercial community. This part of the study was aimed at understanding the high volume market, both commercial and military, and determine the criteria under which HTSC-MCM would be accepted by system producers.

About a year ago, having met with a number of commercial systems houses, we realized that while HTSC-MCM technology held great promise, much development is still needed to achieve the ultimate goals of the program. However, as we got into it in more depth we discovered that the HTSC-MCM foundries could become unstable since their financial backers may not have either the patience and the stamina to wait for this technology and its market to develop. We subsequently recommended that this program should be modified to allow those foundries to consider the possibility of fabricating conventional MCMs but operating them at cryotemperature. This approach has several benefits: (a) Cold CMOS does exhibit significant performance improvement below -100°C; (b) Some companies are already considering the possibility of cooling their systems to gain performance, meaning a near term market could be addressed by the HTSC foundries; (c) These foundries need to develop the cryotechnology anyway, including cryogenic assemblies, cryotesting and packaging, and IC optimization for cryotemperature operation. We consequently crusaded the industry infrastructure to alter the HTSC-MCM program and make it slightly more general. The new program that we recommended should really be cryoelectronics which includes HTSC-MCM, IC optimization and cryogenic cooling, etc. This program received the support of industry, universities, and DARPA. This program indeed becomes more important in light of the finding by SIA that within ten to fifteen years the IC industry will face major challenges if they plan to continue the same rate of on-chip performance and complexity. Not only is the cost of new CMOS foundries reaching exhorbitant levels

($1B per foundry) but now they have to rely on new processing, testing and packaging technologies to reach their goals. The result is an unquestionable high cost in R&D and a significant delay to the marketplace. Cryoelectronics could relieve a great deal of the pressure.

More recently however we reached yet another plateau. It became clear to us that even conventional MCM's are having difficulty being accepted by system houses. We believe the reason for this to be that MCM's are being populated by IC's optimized for single packages and not for MCM's. Initial studies by RC Eden and Doug Paffel clearly showed that if IC's are optimized for MCM's new and major strides can be achieved in the near term. The following is a summary of our findings:

The MCM technology brings in two major features: (1) Wiring densities comparable to those used on chips, and (2) Via pitch transformer capability that can couple the IC to the PCB. With these two features we now can do the following: (a) We can wire chips to each other using extremely high numbers of I/O contacts. This means that in going from one chip to the other, the connectivity does not go through major discontinuity. Interchip interconnect will appear much like the on chip wiring. Therefore if the IC's have area pad I/O we could obviate the dis-economic urge to design very large IC's. Since large IC's are designed to circumvent the constraints of low peripheral IC I/O counts, the combination of IC area I/O and high wiring density MCMs could give the electronics industry the ability to wire many small area-I/O chips on MCMs and make them look as if they are a single jumbo chip. The benefits of this approach are indeed staggering: (a) By using small chips we continue to operate on the high yield part of the yield curve, this means cost per gate can be reduced significantly. (b) Functionality that was compromised out to the peripheral I/O limitation can be reinstated adding an additional factor in performance. (c) Using smaller blocks of chips gives us higher flexibility of using these chips thereby adding to the utility and perhaps product life cycle and (d) Earlier market penetration since smaller chips can then be produced more quickly.

Having said all of the above it now becomes clear that devices optimized not only for cryotemperature operation but also for MCM packaging could lead to performance improvements exceeding 16x and price/performance ratios possibly exceeding 64x. It is for this reason that now we recommend that the HTSC-MCM program should be broadened to include MCM and cryotemperature optimization ranging from room temperature to 80°k. This program should give system houses great incentives to use MCMs over a wide range of temperature operation.

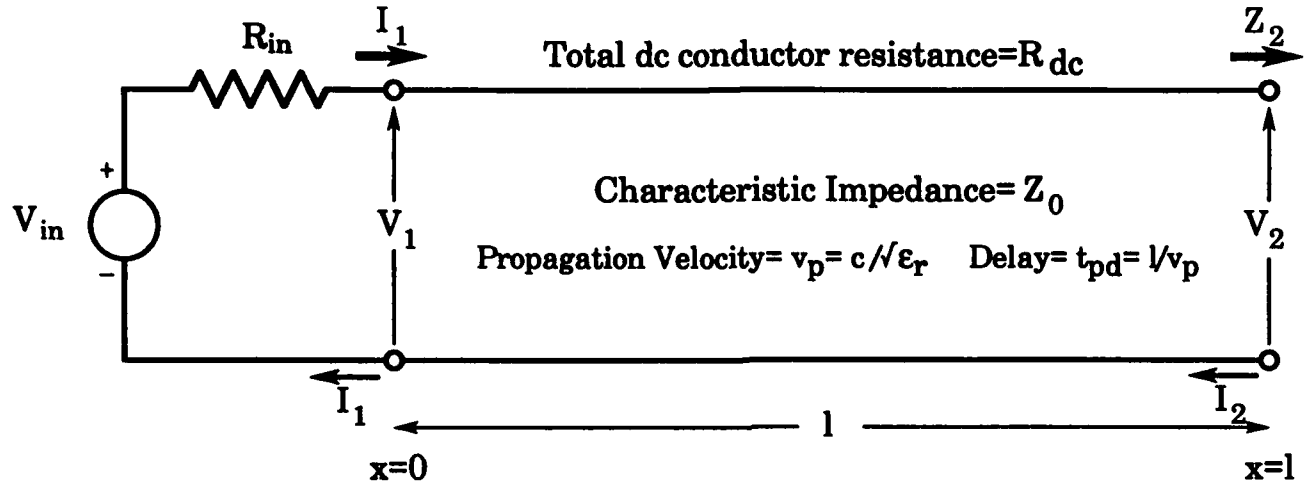
1.3. Source-Terminated Lossy Line Transient Response Characteristics

The principal integrated circuit technology of interest for cyoelectronic applications (with or without HTSC interconnects) is silicon CMOS. Far and away the most common signal interconnection scheme employed with CMOS ICs is the source terminated, open-load transmission line configuration shown in Figure 1.3. While the Fourier transform approach (see Section 2 and 3) for very accurately modeling the transient response of small lossless dielectric lossy conductor transmission line interconnects (eg. as used in MCMs) will work for any signal interconnect system having reasonably linear driver and load characteristics, our focus thus far has been principally on the CMOS-like source terminated open load configuration of Figure 1.3.

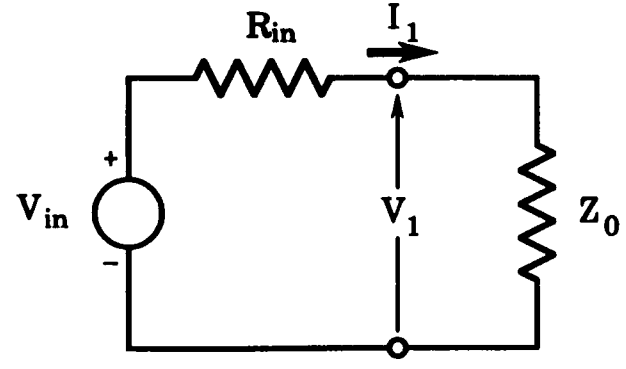
Before presenting the results of the detailed computer modeling of these interconnects, it is worth spending a few minutes effort in trying to understand from an analytical viewpoint. The lossless ($R_{dc} = 0$ and $R_{ac} = 0$) case for the source terminated open load (STOL) configuration of Figure 1.3 is discussed in the last quarterly report (Section 2 of this document), and should best be read before proceeding with this final report material. Note that the material in the last three quarterly reports (Sections 3.2, 3.3 and 2 of this document) is presented as one continuous text, with figure numbers, equation numbers and reference numbers consistent between them (only the reference number continuity is maintained in this final report section).

As shown in Figures 36 through 49 in Section 2, for the lossless (R_{dc} and $R_{ac} = 0$) conductor case, the lossless STOL load end voltage response, V_2, is a sequence of output steps, beginning at $t = \tau_{pd}$ (where τ_{pd} is the one-way preparation delay) each step of duration $2\tau_{pd}$ (the round trip propagation delay). Equations 49 and 51 give the amplitudes of the first two steps ($\tau_{pd} < t < 3\tau_{pd}$ and $3\tau_{pd} < t < 5\tau_{pd}$ respectively). The major pulse distortion effect which is introduced by lossy conductors is caused by the dc series resistance (primarily of the center conductor in

Lossy (dc only†) Transmission Line



Model for initial pulse response at the input for $0<t<2t_{pd}$ (before I_2 reflections arrive back at input):



$$V_1 = \frac{V_{in} Z_0}{R_{in} + Z_0}$$

$$I_1 = \frac{V_{in}}{R_{in} + Z_0}$$

†For simplicity, frequency-dependent skin effect loss is not included here. (It is included in the computer analysis, of course.)

Figure 1.3

coax, as the larger ground plane is lower resistance), R_{dc} in Figure 1.3. The "zero order" approximation to the lossy line response is obtained by noting in Figure 1 that at $t = \tau_{pd}$ there is a current I_1 flowing through a series resistance R_{dc} distributed along the line, and so the output voltage will be reduced by an amount $\Delta V = I_1 R_{dc}$ below that given in Equation 49. This means that to "zero order", the initial load voltage, V_2, should be given by:

$$V_2(t = \tau_{pd}) \approx \frac{2 V_{in} Z_o}{R_{in} + Z_o}\left(1 - \frac{R_{dc}}{2Z_o}\right) \qquad \text{Eq. 1.1}$$

Immediately after $t = \tau_{pd}$, a negative reflected current pulse (I_2 in Figure 1.3) starts back toward the source, which progressively reduces the $(I_1 - I_2)R_{dc}$ ohmic conductor drop on the line. To "zero order", this conductor drop goes to zero when the I_2 pulse gets back to the source, which is seen at $t = 2\tau_{pd}$ at the source, but not until $t = 3\tau_{pd}$ at the load end. Hence, the "zero order" at the load end we see at $t = 3\tau_{pd}^{-}$ (the "-" meaning "just before the ρ_s reflection discontinuity arrives")

$$V_2(t = 3\tau_{pd}^{-}) \approx \frac{2 V_{in} Z_o}{R_{in} + Z_o} \qquad \text{Eq. 1.2}$$

which is the same as the lossless step height of Equation 49. In between $t = \tau_{pd}$ and $t = 3\tau_{pd}^{-}$ the output voltage will, to "zero order" just go linearly between the values given by Equations 1.1 and 1.2, since the I_2 pulse moves at constant velocity, "erasing" the $(I_1 - I_2)R_{dc}$ ohmic voltage drop linearly in time.

These "zero order" expressions are reasonably accurate when R_{dc} is small but do not count the fact that the current along the line must decrease somewhat as the IR_{dc} drop reduces the voltage (since the ratio of voltage to current is Z_o). This simply implies, of course, an exponential decay of the initial pulse height with $R_{dc}/2Z_o$ instead of the linear decay of Equation 1.1. Hence, to first order (as shown for $R_{in} = Z_o$ in Equation 7, Section 3.2) we have the output voltage at $t = \tau_{pd}$ given for R_{dc} (only) loss by:

$$V_2(t = \tau_{pd}) = \frac{2V_{in}Z_o}{R_{in}+Z_o}\, e^{-\frac{R_{dc}}{2Z_o}} \qquad \text{for } R_{dc} \text{ (only)} \qquad \text{Eq. 1.3}$$

The various current reflections which make Equation 1.3 different from eq. 1.1 do not all die out completely at $t = 3\tau_{pd}$, so that (simply updating Equation 8 for the $R_{in} \neq Z_o$ general case) we will have at $t = 3\tau_{pd}^{-}$,

$$V_2(t = 3\tau_{pd}^{-}) = \frac{2V_{in}Z_o}{R_{in}+Z_o}\, e^{-0.48\left(\frac{R_{dc}}{2Z_o}\right)^2} e^{-\left(\frac{R_{dc}}{2Z_o}\right)} \qquad \text{for } R_{dc} \text{ (only)} \qquad \text{Eq. 1.4}$$

In the lossless and R_{dc}(only) lossy transient response characteristics, the step response is marked by discontinuities in output voltage, V_2, at $t = \tau_{pd}, 3\tau_{pd}, 5\tau_{pd}$, etc. These "zero risetime" output steps are an artifact of the zero risetime of the input and the infinite bandwidth assumed for the transmission line because we have ignored the skin effect losses on the conductors (primarily the center conductor in coaxial lines). When skin effect loss is included (eg., see Subsection 1.2.3, Pages 1-9 to 1-13 and Figure 1 of Section 3.2, Equations 9-23) there abrupt transitions are shown to have a finite risetime and a complementary error function shape (Equations 14 and 15 and Figures 2 through 6). A practical approach for including both the R_{dc} and skin effect loss characteristics in an analytical model was given in Subsection 1.2.5, Pages 1-15 through 1-17 and Figures 7 through 15.

These analytic approximations handle reasonably low loss lines fairly accurately except in the "tail" region (approaching asymptotic response), where small errors tend to accrue. This is also the case for the Quad Design XNS tools (which is quite satisfactory for the engineering design application for which these tools are intended, where a 1-2 percent error in the far tail response is not of consequence in digital circuits). However, for highly lossy and very small lines, some of the approximations in standard analyses are inadequate and place the accuracy of the resulting transient responses in question. The intent of the effort described in detail in Section 3.3 was to model these extreme cases with a high degree of accuracy (but limited to linear drivers and not having as fast run-times as needed for commercial engineering tools). Because skin effect can be easily modeled in the frequency domain, the analysis is done initially in the frequency domain, and then an inverse Fourier transform (8192 point) is carried out to produce the time domain impulse response, which is subsequently integrated to give the step response. While small copper coax lines were modeled in this work so that analytical expressions (using the *ber* and *bei* Kelvin functions given in Equations 40 and 41) for the ac series resistance and internal inductance of the center conductor are known, other geometries could be modeled using the approximations given in Section 2.4 of Reference 5. In the analysis, both the characteristic impedance, Z_o, and the propagation constant, γ, are taken as complex, frequency dependent quantities. The analysis was done using the Bimillenium "HiQ" engineering/scientific software package, running wither on a Macintosh fx or a Powerbook 170 computer. The step response results are stored as an 8192 point vector and are analyzed and plotted using Microsoft EXCEL. Because EXCEL 4.0 cannot handle more than 4000 points in a plot, it was necessary, in order to plot "full time span" results like those in Figures 1.4, 1.6, 1.9 etc., to create a second 4096 point output file (skipping every other data point in the 8192 point file). The expanded time scale plots (Figures 1.5, 1.7, 1.10, etc.) were made from the original 8192 point files for the best time resolution (4ps in Figures 1.4 through 1.16 and 2ps in Figures 1.17 through 1.26, except for Figures 1.6 through 1.8 which are a 2.5ps step size).

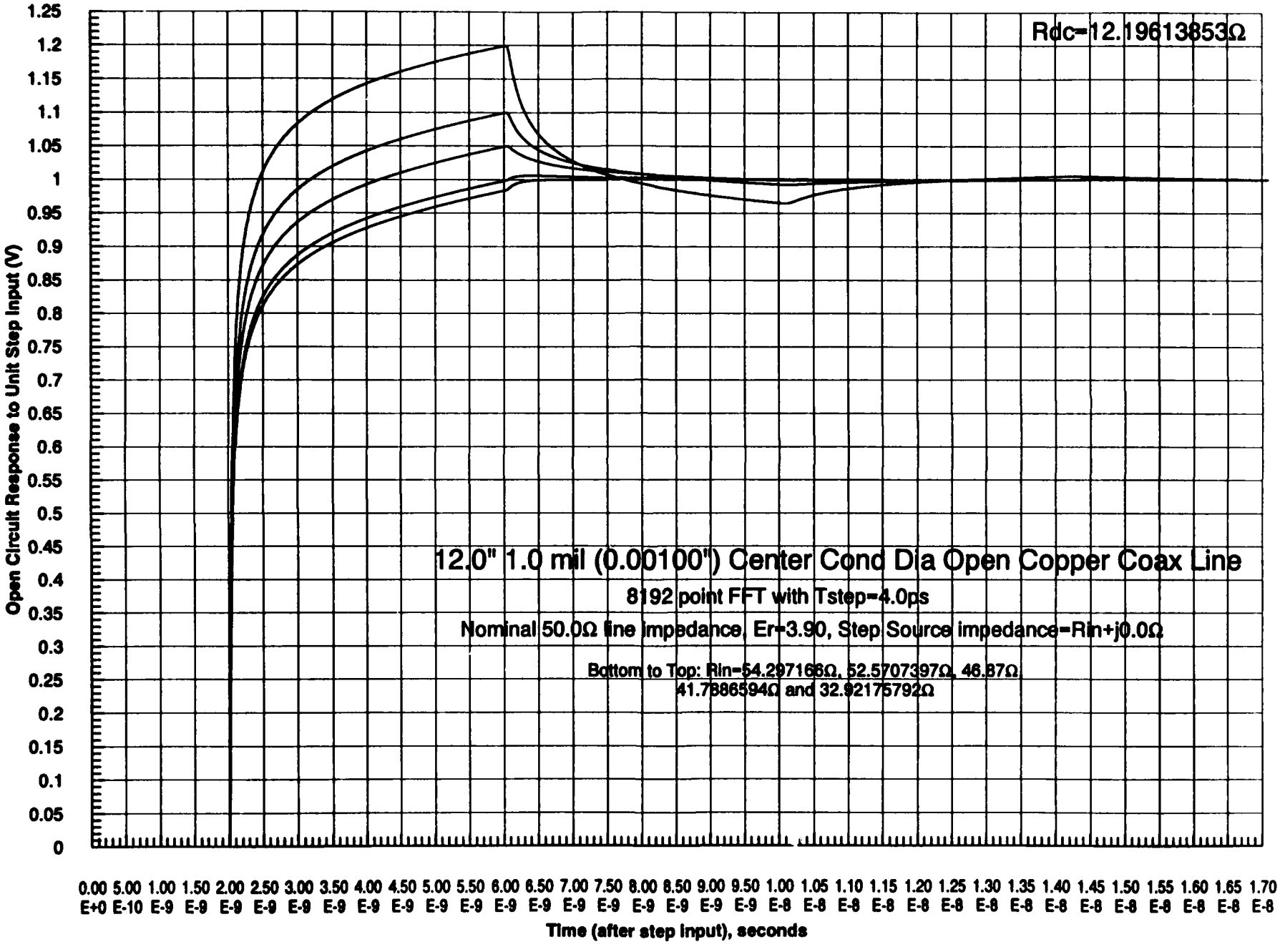

Rdc=12.19613853Ω
12.0" 1.0 mil (0.00100") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=4.0ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=54.297166Ω, 52.5707397Ω, 46.87Ω
41.7886594Ω and 32.921757Ω
Open Circuit Response to Unit Step Input (V)
1.25 1.2 1.15 1.1 1.05 1 0.95 0.9 0.85 0.8 0.75 0.7 0.65 0.6 0.55 0.5 0.45 0.4 0.35 0.3 0.25 0.2 0.15 0.1 0.05 0
0.00 E+0 5.00 E-10 1.00 E-9 1.50 E-9 2.00 E-9 2.50 E-9 3.00 E-9 3.50 E-9 4.00 E-9 4.50 E-9 5.00 E-9 5.50 E-9 6.00 E-9 6.50 E-9 7.00 E-9 7.50 E-9 8.00 E-9 8.50 E-9 9.00 E-9 9.50 E-9 1.00 E-8 1.05 E-8 1.10 E-8 1.15 E-8 1.20 E-8 1.25 E-8 1.30 E-8 1.35 E-8 1.40 E-8 1.45 E-8 1.50 E-8 1.55 E-8 1.60 E-8 1.65 E-8 1.70 E-8
Time (after step input), seconds

Figure 1.4

1.4. Small Lossy Coax Transient Response Simulation Results for Fixed Overshoots

A key question in MCM technology is what is the maximum allowable line resistance (dc or ac) for the signal interconnects. For example, in References 5 and 6 a R_{MAX} + 10Ω value was taken for the maximum conductor resistance for most cases, or R_{MAX} = 25Ω considered for so called "self-terminated lines" (see discussion by Equations 50 and 51). One question is up to what frequency the conductor resistance should be kept to R_{MAX} for signals of a given risetime. Another question is how effectively the distributed ohmic dc or skin effect resistance can be compensated by reduction in R_{in} (the source termination resistance at the driver). Also, what would happen to the voltage waveforms if all output drivers had the same reduced R_{in} values, even if they were driving shorter, lower resistance lines. The answers to these questions allow us to determine how small the copper signal lines may be made for a given size and performance level MCM.

In Section 2, 12" long 300°K copper coax lines (eg., longest lines on a 6" MCM) were analyzed with center conductor diameters of 1.0 mils, 0.5 mils and 0.25 mils, for a range of R_{in} values (eg., 30Ω , 35Ω, 40Ω, 45Ω, 50Ω and 55Ω in Figures 50 and 51). Also, one 6" line length case with a 0.5 mils center conductor diameter and a similar range of R_{in} values was presented. In this section, simulation results are presented for a full matrix of line lengths and center conductor diameters. Specifically, diameters of 1.0 mils, $1/\sqrt{2}$ mils (0.7071 mils), 0.5 mils, $1/2\sqrt{2}$ mils (0.3535 mils) and 0.25 mils are analyzed in line lengths of 12.0" (30.48 cm) and 6.0" (15.24 cm). The $\sqrt{2}$ stepping of center conductor diameters was done to give a factor of 2 stepping in R_{dc} between the various cases.

The other major difference in the simulations of Figures 1.4 through 1.26 is the way in which the driver source resistance, R_{in} was selected for the various curves. The focus is on illuminating how helpful the self-termination approaches can be in allowing (by reducing R_{in}) lines that would otherwise have unacceptably poor

response (due to excessive series resistance) to be used in digital applications. In general, good digital design has some specified "budget" for line aberrations such as overshoot, undershoot, "ringing", etc., just as it has for crosstalk and other factors which eat into the total noise margin budget. A typical number might be a 5% or 10% allowance for overshoot, depending on the IC technology. Hence, in these figures, curves are presented for selected R_{in} values which give peak overshoot values of +20%, +10%, and +5% (as defined in Equation 50), along with one or more curves at near zero overshoot. The latter is difficult, because in the < 1% overshoot region, a lot of subtities in the accurate transient waveforms arise (principally due to the complex, frequency dependent Z_o) which make, for example, the R_{in} for an overshoot of +0.6% quite different than the R_{in} to give a 0.05% overshoot. (This is because the point of peak overshoot moves away from $t = 3\tau_{pd}$, as assumed for the lossless case in Figures 37 and 38). You can see these effects in Figures 1.11, 1.14 and 1.25 particularly.

For the lossless case (eg. Equations 49 and 50 or Figures 37 and 38), for a nominal $Z_o = 50\Omega$, an overshoot of 0% would be obtained with $R_{in} = 50\Omega$, +5% with $R_{in} = 45.238095238\Omega$, +10% overshoot with $R_{in} = 40.9090909\Omega$ and +20% with $R_{in} = 33.333333\Omega$. For cases with low values of R_{dc}, such as the 6.0" 1.0 mil center conductor diameter case of Figures 1.17 and 1.18 ($R_{dc} = 6.098\Omega$), $R_{in} = 34.16177\Omega$ gave +20% overshoot, $R_{in} = 42.65544\Omega$ gave +10%, and $R_{in} = 47.52196\Omega$ gave +5% overshoot. These R_{in}values are close to those predicted for the lossless case. This is not the case for near zero overshoot. For example, a value of $R_{in} = 53.008924\Omega$ gives an overshoot of +0.962% (at $\tau = 3.186$ns and $R_{in} = 62.000\Omega$ gives an overshoot of +0.01315% (at $\tau = 7.450$ ns), whereas in the lossless analysis not including the complex Z_o any R_{in} over 50Ω would be underdamped (negative overshoot).

Two different sets of analysis runs were made for the 12" long, 1.0 mil center conductor diameter case, the first (Figures 1.4 and 1.5) at a $\tau_{step} = 4$ps step size (after ifft), and the second (Figures 1.6 and 1.7, summarized in Figure 1.8) at a 2.5ps

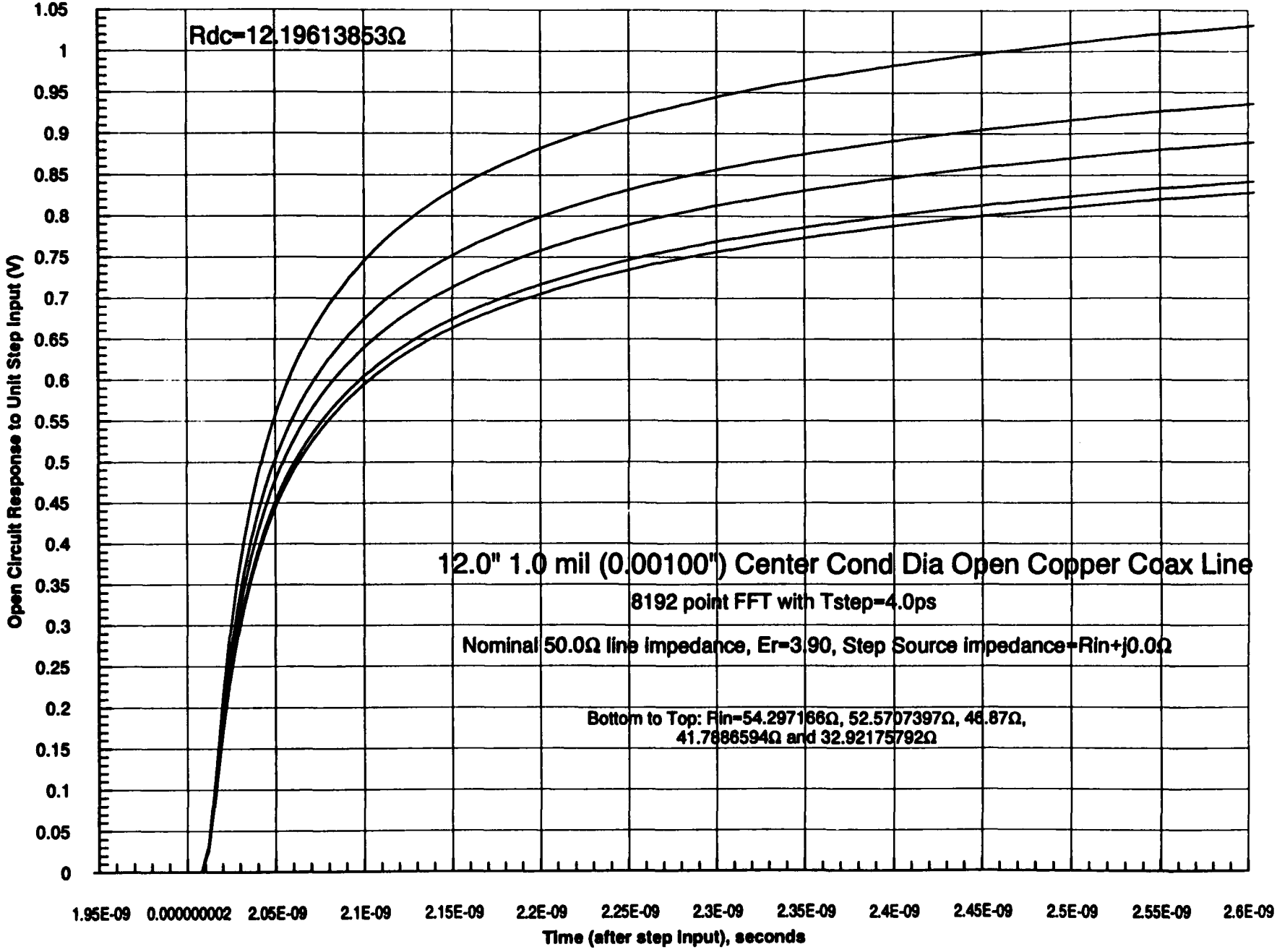

Rdc=12.19613853Ω
12.0" 1.0 mil (0.00100") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=4.0ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=54.297166Ω, 52.5707397Ω, 46.87Ω,
41.7886594Ω and 32.92175792Ω
Open Circuit Response to Unit Step Input (V)
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
1.95E-09
0.000000002
2.05E-09
2.1E-09
2.15E-09
2.2E-09
2.25E-09
2.3E-09
2.35E-09
2.4E-09
2.45E-09
2.5E-09
2.55E-09
2.6E-09
Time (after step input), seconds

Figure 1.5

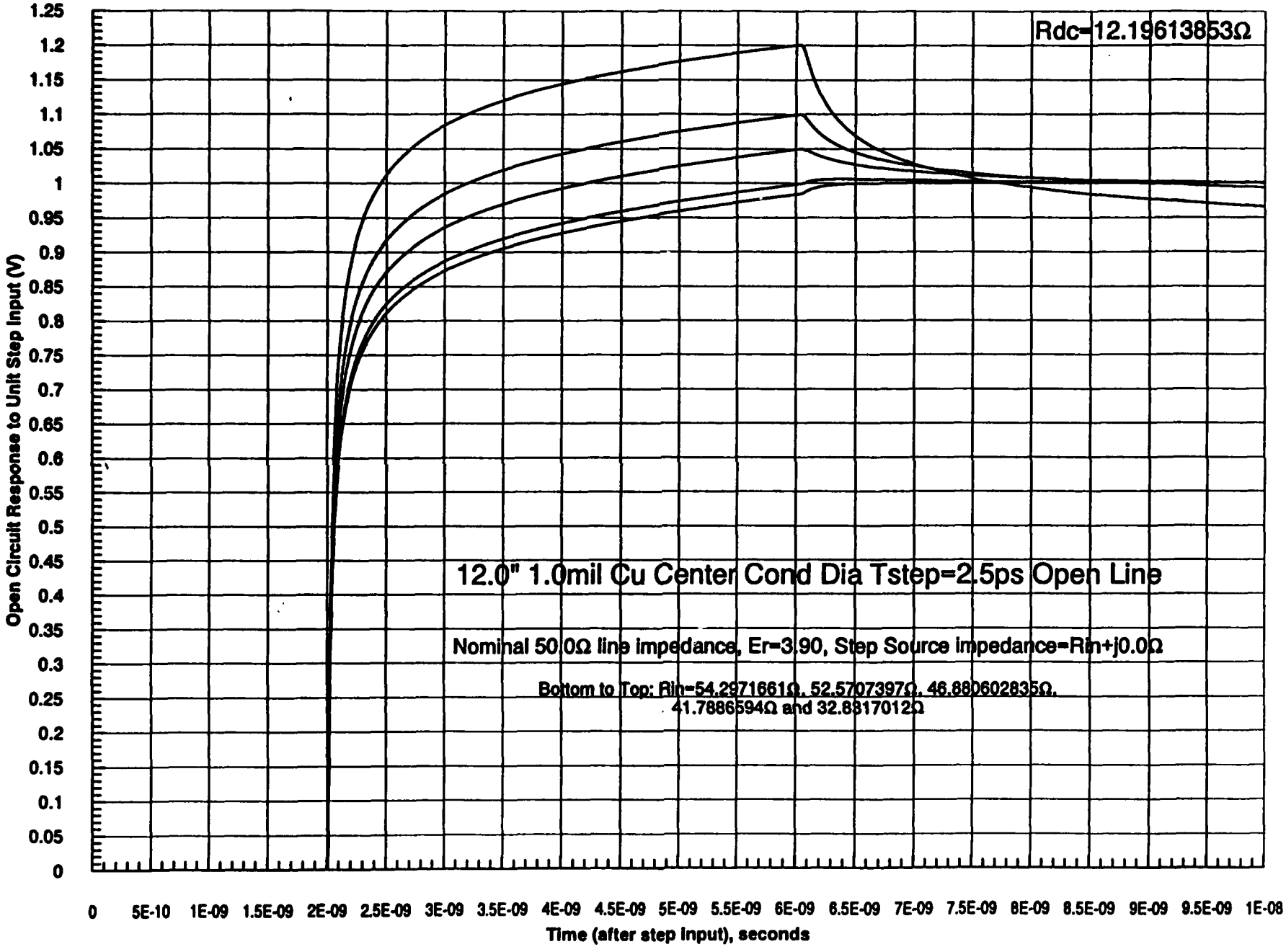

Rdc=12.19613853Ω
12.0" 1.0mil Cu Center Cond Dia Tstep=2.5ps Open Line
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=54.29716610Ω, 52.57073970Ω, 46.88060283Ω,
41.78865940Ω and 32.88170120Ω
Open Circuit Response to Unit Step Input (V)
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0
5E-10
1E-09
1.5E-09
2E-09
2.5E-09
3E-09
3.5E-09
4E-09
4.5E-09
5E-09
5.5E-09
6E-09
6.5E-09
7E-09
7.5E-09
8E-09
8.5E-09
9E-09
9.5E-09
1E-08
Time (after step input), seconds

Figure 1.6

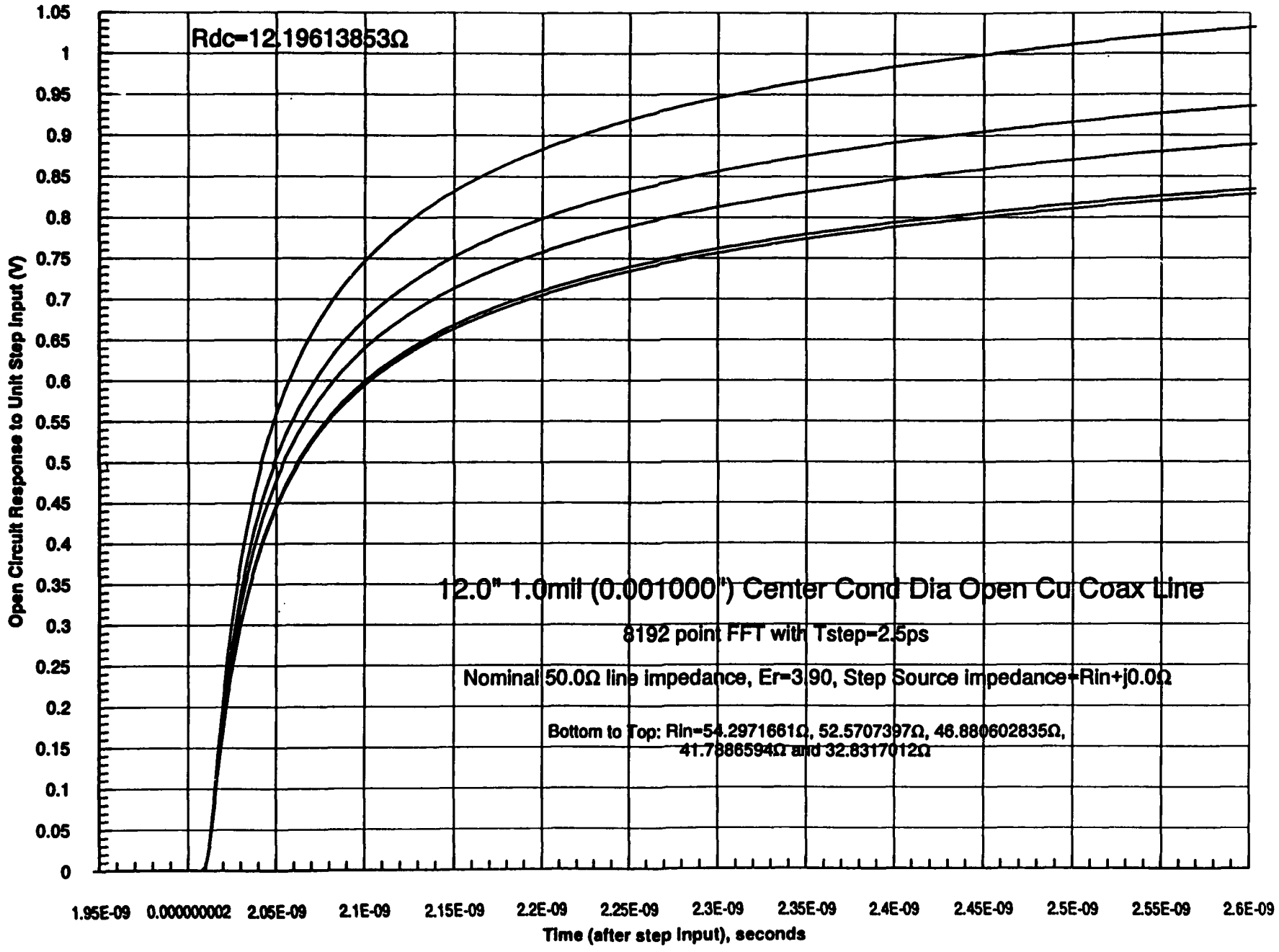

Rdc=12.19613853Ω
12.0" 1.0mil (0.001000") Center Cond Dia Open Cu Coax Line
8192 point FFT with Tstep=2.5ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=54.2971661Ω, 52.5707397Ω, 46.8806028 35Ω,
41.7886594Ω and 32.8317012Ω
Open Circuit Response to Unit Step Input (V)
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
1.95E-09
0.000000002
2.05E-09
2.1E-09
2.15E-09
2.2E-09
2.25E-09
2.3E-09
2.35E-09
2.4E-09
2.45E-09
2.5E-09
2.55E-09
2.6E-09
Time (after step input), seconds

Figure 1.7

0%, +5%, +10% & +20% OverShoot Summary V2Int vs. t for 12" 1.0 mil center cond dia Cu Coax (300°K)

R. C. Eden 9/2/92 HiQ 8192 pt iFFT Tstep=2.5ps LossyLine Calcs

Overshoot=	0.0%; Rin(Ω)=	+5.0%; Rin(Ω)=	+10.0%; Rin(Ω)=	+20.0%; Rin(Ω)=	+0.2%; Rin(Ω)=	+0.6%; Rin(Ω)=
Crossing Amplitude	54.29716609	46.88060284	41.7886594	32.8317012	53.54128093	52.5707397
First or [Last]						
1%	2.0105892E-09	2.0105191E-09	2.0104700E-09	2.0103556E-09	2.0105820E-09	2.0105728E-09
2%	2.0115781E-09	2.0114379E-09	2.0113406E-09	2.0111415E-09	2.0115638E-09	2.0115454E-09
5%	2.0136506E-09	2.0134533E-09	2.0133172E-09	2.0130622E-09	2.0136304E-09	2.0136046E-09
10%	2.0163399E-09	2.0159710E-09	2.0157171E-09	2.0160605E-09	2.0163023E-09	2.0162540E-09
20%	2.0220968E-09	2.0212029E-09	2.0205882E-09	2.0195449E-09	2.0220057E-09	2.0218887E-09
50%	2.0630901E-09	2.0543414E-09	2.0493102E-09	2.0419063E-09	2.0621058E-09	2.0608844E-09
80%	2.4490201E-09	2.2719474E-09	2.2015423E-09	2.1278591E-09	2.4250488E-09	2.3966411E-09
90%	3.4029187E-09	2.6747436E-09	2.4305541E-09	2.2214289E-09	3.2987856E-09	3.1768784E-09
95%	4.6741347E-09	3.1845104E-09	2.6923991E-09	2.3089113E-09	4.4679789E-09	4.2217843E-09
98%	5.8454123E-09	3.7105637E-09	2.9533537E-09	2.3864147E-09	5.5775529E-09	5.2454519E-09
99%	6.1137545E-09	3.9405053E-09	3.0666029E-09	2.4182465E-09	6.0077538E-09	5.6532066E-09
[101%-99%]		7.6665697E-09	7.8318580E-09	1.1248861E-08		
[102%-98%]		6.8186500E-09	7.2188165E-09	1.0619031E-08		
[105%-95%]			6.4176915E-09	6.6804606E-09		
[110%-90%]				6.3125308E-09		
Risetime Data:						
20%-80%	4.2692331E-10	2.5074449E-10	1.8095403E-10	1.0831420E-10	4.0304313E-10	3.7475244E-10
10%-90%	1.3865789E-09	6.5877265E-10	4.1483706E-10	2.0536836E-10	1.2824833E-09	1.1606244E-09
5%-95%	2.6604841E-09	1.1710571E-09	6.7908187E-10	2.9584913E-10	2.4543484E-09	2.2081797E-09
2%-98%	3.8338341E-09	1.6991258E-09	9.4201309E-10	3.7527323E-10	3.5659891E-09	3.2339065E-09
1%-99%	4.1031654E-09	1.9299862E-09	1.0561329E-09	4.0789087E-10	3.9971718E-09	3.6426338E-09

Figure 1.8

step size. The results were virtually identical for the two analyses. For example, with R_{in} = 41.7886594Ω, the 2.5ps run gave an overshoot of 10.0000817% at 6.040ns and the 4ps run gave 9.9987777% at 6.040ns, only a 20.4$\mu\gamma$ difference in peak output in a 1 volt pulse amplitude. Additional verification of the accuracy of the calculations is the fact that there is virtually zero output seen at V_2 prior to the nominal pulse arrival time, $\tau_{pd} = l\,v_\rho$ (where $v_\rho = c/\sqrt{\varepsilon_r} = 1.518 \times 10^8$meters/s for the $\varepsilon_r = 3.90$ dielectric constant assumed, or $1/v_\rho$ = 167.3ps/inch). For l = 12", τ_{pd} = 2.007ns, or for a l = 6" line length, τ_{pd} = 1.00ns. Note in the most expanded time scale l = 12" plot, Figure 1.7, the extrapolated pulse arrival time is indeed 2.0075ns (the 2.0075ns step showing zero output and the next time point at 2.010ns showing finite output). Another measure of the accuracy of the calculation is the fact that while the original calculation is done in the frequency domain, (inverse) Fourier transformed to the time domain impulse response, with the result integrated to give the step response, without any amplitude or slope correction the asymptotic pulse amplitude goes precisely to 1.00000000 volt. This accuracy is due in part to the numerical precision of the Bimillenium HiQ software, coupled with care in getting the physics into the problem correctly (ie., being very careful that the frequency domain pin-phase characteristics do not violate the Kramers-Kronig relationship) and avoiding approximations which would induce artifacts into the output.

As mentioned previously, in digital systems it is a common design approach to assign a specific overshoot/undershoot budget as part of the overall noise margin budget. This differs from the peak overshoot value in that it represents the actual signal error at the time the logic decision is made. The peak overshoot value may lead to improper circuit function or even degraded IC reliability. The error budget concerns the accuracy of the decision process (in analogy to the signal settling time in an analog circuit or A/D). As seen in Figures 1.4 through 1.26, in this source-terminated, open-load configuration (Figure 3), substantial improvements in signal risetime at the end of lossy lines can be achieved by reducing the driver resistance, R_{in} below the normal $R_{in} = Z_o$ value to compensate for the ohmic line resistance. It is important to note, however, that reducing R_{in} may in fact lengthen

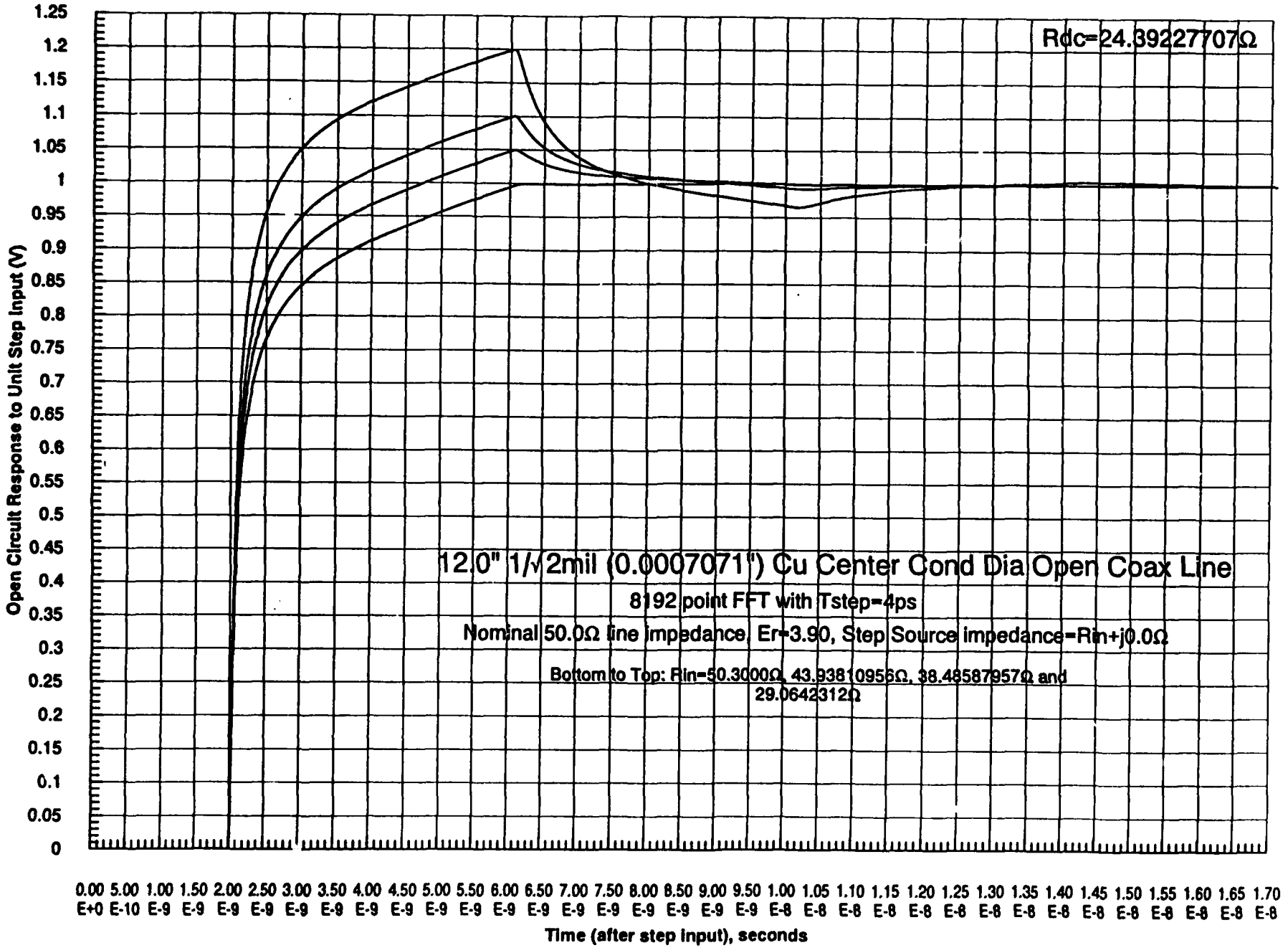

Rdc=24.39227707Ω
12.0" 1/√2mil (0.0007071") Cu Center Cond Dia Open Coax Line
8192 point FFT with Tstep=4ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=50.3000Ω, 43.93810956Ω, 38.48587957Ω and 29.06423120Ω
Open Circuit Response to Unit Step Input (V)
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0.00 E+0
5.00 E-10
1.00 E-9
1.50 E-9
2.00 E-9
2.50 E-9
3.00 E-9
3.50 E-9
4.00 E-9
4.50 E-9
5.00 E-9
5.50 E-9
6.00 E-9
6.50 E-9
7.00 E-9
7.50 E-9
8.00 E-9
8.50 E-9
9.00 E-9
9.50 E-9
1.00 E-8
1.05 E-8
1.10 E-8
1.15 E-8
1.20 E-8
1.25 E-8
1.30 E-8
1.35 E-8
1.40 E-8
1.45 E-8
1.50 E-8
1.55 E-8
1.60 E-8
1.65 E-8
1.70 E-8
Time (after step input), seconds

Figure 1.9

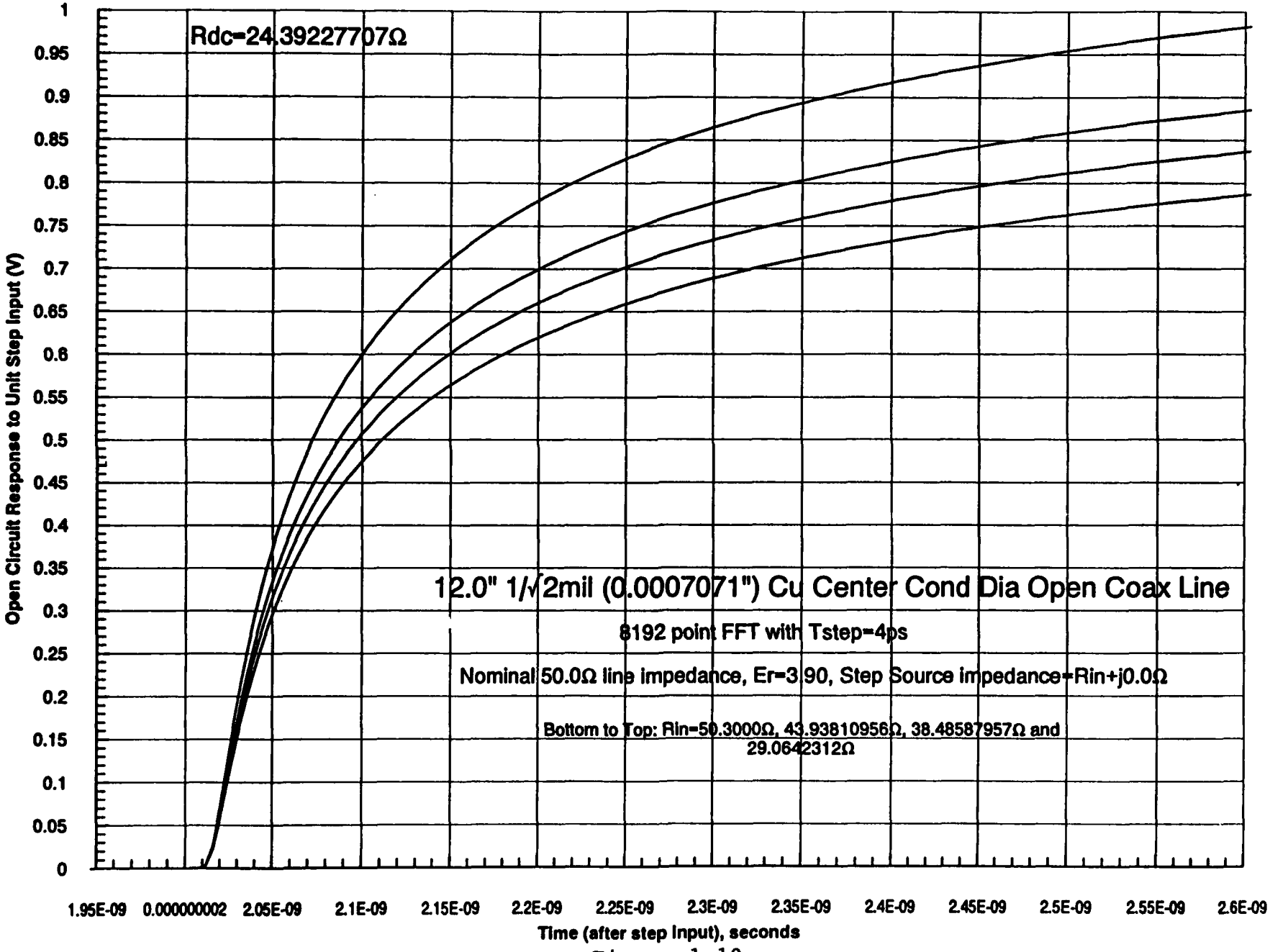

Rdc=24.39227707Ω
12.0" 1/√2mil (0.0007071") Cu Center Cond Dia Open Coax Line
8192 point FFT with Tstep=4ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=50.3000Ω, 43.93810956Ω, 38.48587957Ω and 29.0642312Ω
Open Circuit Response to Unit Step Input (V)
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
1.95E-09
0.000000002
2.05E-09
2.1E-09
2.15E-09
2.2E-09
2.25E-09
2.3E-09
2.35E-09
2.4E-09
2.45E-09
2.5E-09
2.55E-09
2.6E-09
Time (after step Input), seconds

Figure 1.10

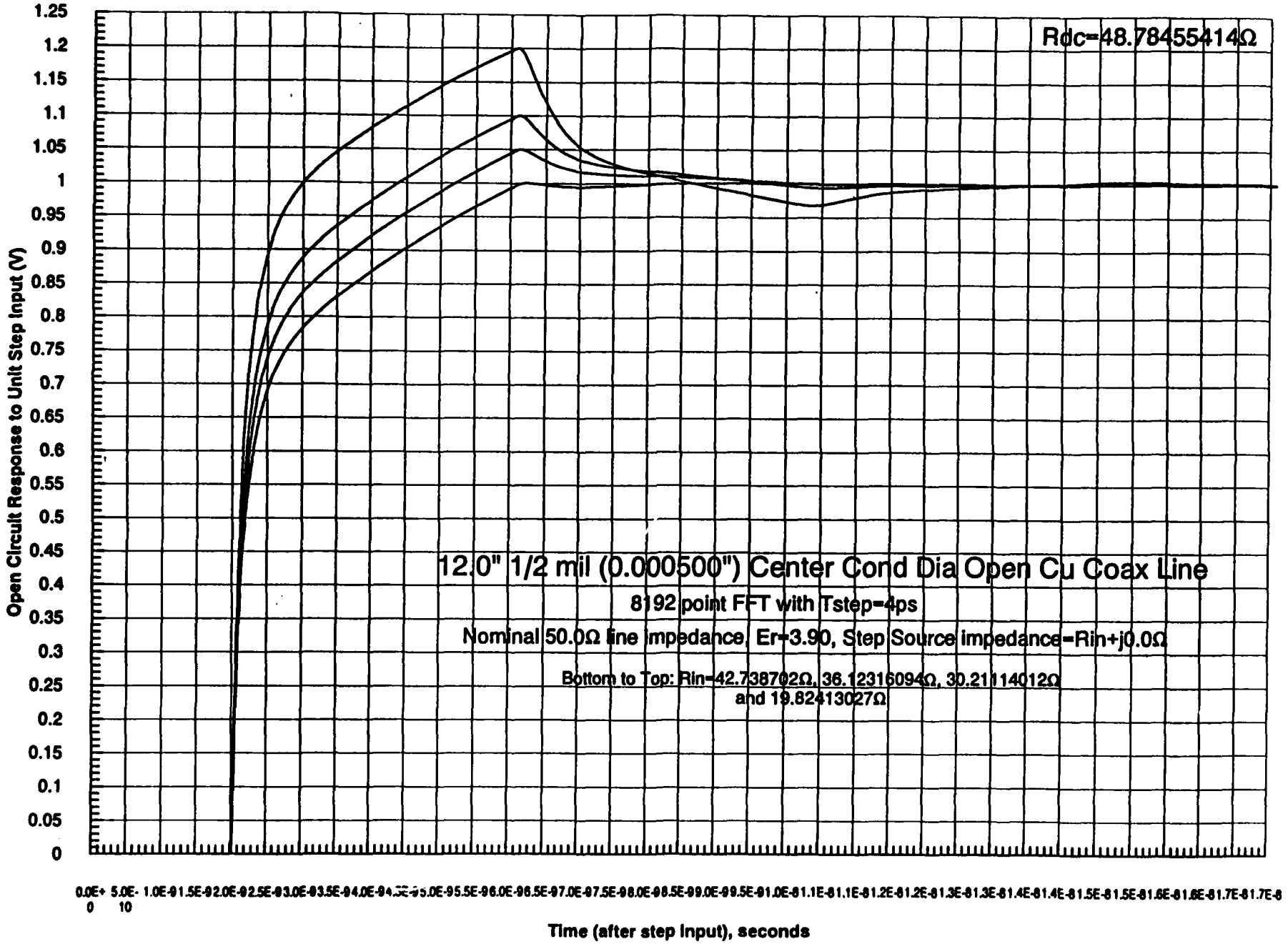

Rdc=48.78455414Ω
12.0" 1/2 mil (0.000500") Center Cond Dia Open Cu Coax Line
8192 point FFT with Tstep=4ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=42.738702Ω, 36.12316094Ω, 30.21114012Ω
and 19.82413027Ω
Open Circuit Response to Unit Step Input (V)
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0.0E+0
5.0E-10
1.0E-9
1.5E-9
2.0E-9
2.5E-9
3.0E-9
3.5E-9
4.0E-9
5.0E-9
5.5E-9
6.0E-9
6.5E-9
7.0E-9
7.5E-9
8.0E-9
8.5E-9
9.0E-9
9.5E-9
1.0E-8
1.1E-8
1.1E-8
1.2E-8
1.2E-8
1.3E-8
1.3E-8
1.4E-8
1.4E-8
1.5E-8
1.5E-8
1.6E-8
1.6E-8
1.7E-8
1.7E-8
Time (after step input), seconds

Figure 1.11

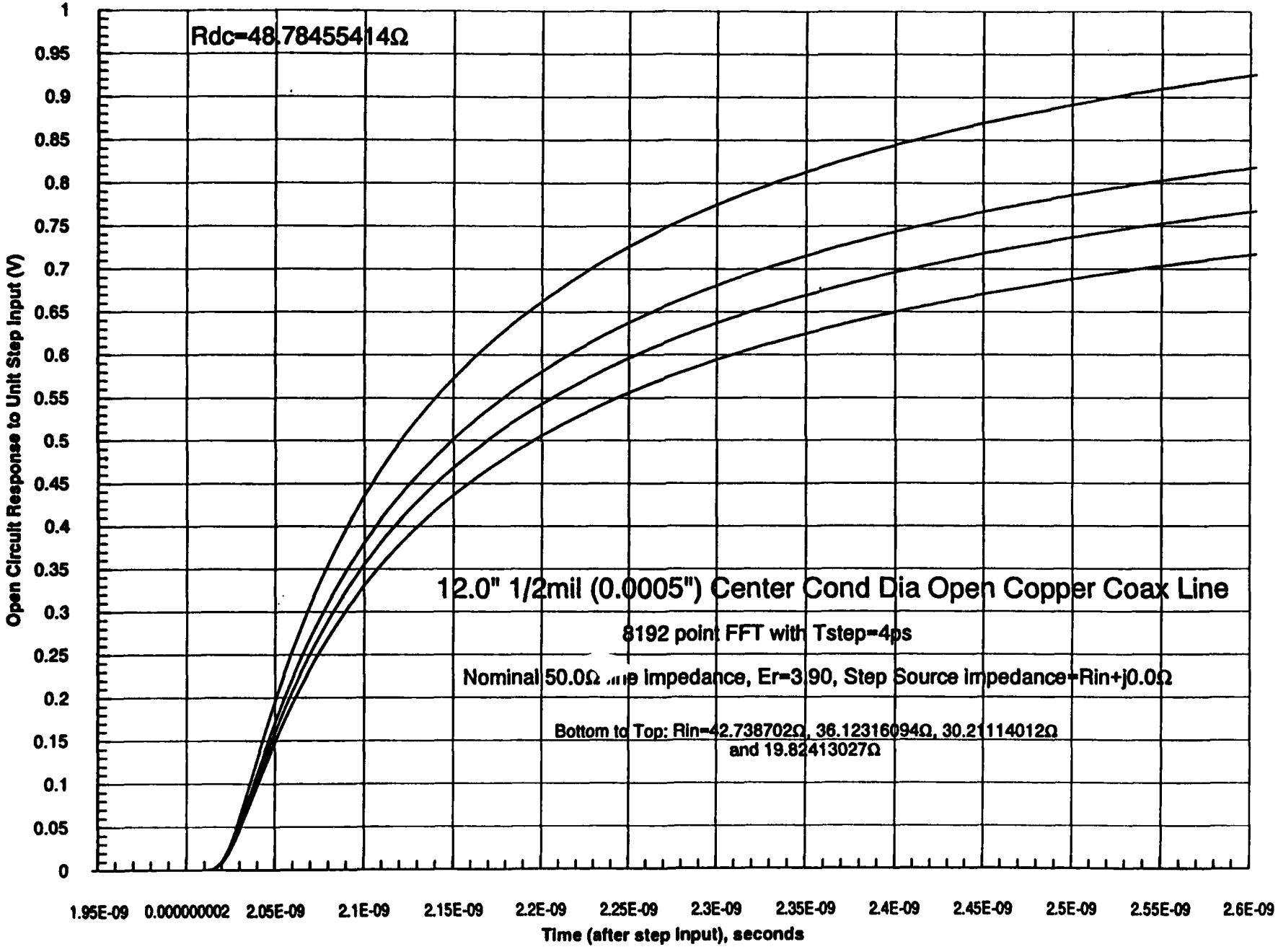

Rdc=48.784554 14Ω
12.0" 1/2mil (0.0005") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=4ps
Nominal 50.0Ω ...e impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=42.738702Ω, 36.12316094Ω, 30.21114012Ω
and 19.82413027Ω
Open Circuit Response to Unit Step Input (V)
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
1.95E-09
0.000000002
2.05E-09
2.1E-09
2.15E-09
2.2E-09
2.25E-09
2.3E-09
2.35E-09
2.4E-09
2.45E-09
2.5E-09
2.55E-09
2.6E-09
Time (after step input), seconds

Figure 1.12

0%, +5%, +10% & +20% OverShoot Summary V2Int vs. t for 12" 0.5000 mil center cond dia Cu Coax (300°K)

R. C. Eden 9/12/92 HiQ 8192 pt iFFT Tstep=4.0ps LossyLine Calcs

Overshoot= Crossing Amplitude First or [Last]	0.0%; Rin(Ω)= 42.738702	+5.0%; Rin(Ω)= 36.12316094	+10.0%; Rin(Ω)= 30.21114012	+20.0%; Rin(Ω)= 19.82413027
1%	2.0208248E-09	2.0205905E-09	2.0203810E-09	2.0200122E-09
2%	2.0240942E-09	2.0236617E-09	2.0232432E-09	2.0225071E-09
5%	2.0308262E-09	2.0300968E-09	2.0294447E-09	2.0282977E-09
10%	2.0405396E-09	2.0391848E-09	2.0379792E-09	2.0358561E-09
20%	2.0615504E-09	2.0583014E-09	2.0554842E-09	2.0507652E-09
50%	2.1954044E-09	2.1693202E-09	2.1494821E-09	2.1208316E-09
80%	3.1631200E-09	2.7563115E-09	2.5405167E-09	2.3315303E-09
90%	4.4575642E-09	3.7208779E-09	3.1102243E-09	2.5230382E-09
95%	5.2483310E-09	4.4201032E-09	3.6837803E-09	2.6987018E-09
98%	5.7709346E-09	4.8834926E-09	4.0933887E-09	2.8625912E-09
99%	5.9541167E-09	5.0457011E-09	4.2377759E-09	2.9326021E-09
[101%-99%]		8.3640690E-09	8.8611212E-09	1.1775837E-08
[102%-98%]		6.8589758E-09	7.8084714E-09	1.1012078E-08
[105%-95%]			6.6874822E-09	7.0483308E-09
[110%-90%]				6.6008622E-09
Risetime Data:				
20%-80%	1.1015696E-09	6.9801003E-10	4.8503252E-10	2.8076518E-10
10%-90%	2.4170247E-09	1.6816931E-09	1.0722451E-09	4.8718212E-10
5%-95%	3.2175049E-09	2.3900064E-09	1.6543356E-09	6.7040413E-10
2%-98%	3.7468404E-09	2.8598308E-09	2.0701454E-09	8.4008409E-10
1%-99%	3.9332919E-09	3.0251107E-09	2.2173949E-09	9.1258993E-10

Figure 1.13

the "settling time" necessary to get the signal amplitude within a specified error range. Some of these timing relationships are illustrated for the 12" 1.0 mil center conductor case in Figure 1.8, and for the 12" 0.5 mil case in Figure 1.13. The most common risetime specifications are for 10% to 90% or 20% to 80% of final signal amplitude values. For the 12" 1.0 mil case, the 10% to 90% risetime value with 0% overshoot is 1.387ns, or 69% of the nominal delay time, which value is halved to 0.6588ns (32.8% of τ_{pd}) by reducing R_{in} to 46.9Ω to give a 5% peak overshoot, or even cut to 205.4ps if R_{in} is reduced to 32.8Ω for a 20% overshoot. The problems with this latter, 20% overshoot case, noted in the row with the [110% - 90%] last crossing amplitude entry in the left column, even if the decision error budget were ±10%, the "setting time" would be 6.3125ns, and because of the ringing undershoot, if the budget were a tighter 2% value (shown in the [102% - 98%] row for the +20% column), we would have to wait 10.62ns for the signal to recover to above 98% of final value (as can be seen in Figure 1.4). Such tight error budgets (eg. 1% to 2% or less) are typically associated with A/D conversion as threshold decision circuits, values of 5% or possibly 10% would be more common in all digital designs. However, remember that this 12" 1.0 mil case with a total dc line resistance of 12.2Ω would be considered a good high quality signal line in MCM use. Any shorter lines which used the same R_{in} value, as noted previously, would have larger peak error budgets.

Of particular interest is the case of lines in the "self-terminating" region, with R_{dc} values not small in comparison to Z_o. Figure 1.13 shows this same detailed timing data for the case of a 12" long line with a 0.5 mil center conductor diameter which has R_{dc} = 48.78Ω. As seen in Figure 52, with a nominal $R_{in} = Z_o$ = 50Ω value, the 10% to 90% risetime is a dismal 5.3ns (2.6 times) the propagation delay. If we reduce R_{in} to 42.7Ω for a 0% overshoot, the 10% - 90% risetime improves to 2.417ns (still 1.2 times τ_{pd}) or if we further reduce R_{in} to 36.12Ω for a 5% peak overshoot we can get a 1.68ns risetime (still 84% of τ_{pd}). Note that, as seen in Figure 38, shorter lines with this R_{in} could have up to a 16% overshoot, which could well be acceptable. If more radical reductions in R_{in} are made, such as to R_{in} = 30.2Ω for a 10%

overshoot, the 10%-90% risetime (1.07ns) approaches half of τ_{pd}, but the peak overshoot on shorter lines with this R_{in} would approach 25% which might not be acceptable. As seen in Figure 1.12, the risetime can be reduced to 487ps by dropping R_{in} to 19.842Ω, giving a 20% peak overshoot, but if this R_{in} value were used for shorter lines, the peak overshoot could be severe, up to 43% (Equation 1.2) with heavy ringing (eg., like Figure 48).

While the risetime degradation is serious and pulse overshoot can be severe if constant R_{in} is used on all drivers, clearly (Figures 1.9 through 1.13) reduced R_{in}, "self terminated line" interconnect approaches could be useable for some digital applications in the R_{dc} = 25Ω to 50Ω range ($R_{dc} = Z_o/2$ to Z_o), using R_{in} values in the 25Ω to 40Ω range. If the wire diameter is reduced another factor of 2 however, as shown in the 12" 0.25 mil center conductor diameter case of Figure 1.16, even reducing R_{in} to zero will not bring this R_{dc} = 195Ω case to near critical damping. Even with an R_{in} = 30Ω source resistance, the 90% point of signal response in not reached until nearly 8ns after nominal pulse arrival (4 times τ_{pd}). As seen for l = 6.0" in Figures 1.25 and 1.26, in shorter lines, such small (1/4 mil) copper conductor diameter offers some hope, but even a R_{in} = 25Ω value will not bring the $\tau = 3\,\tau_{pd}$ value up to a positive overshoot, and a negative drive resistance (R_{in} = -2.7107Ω, which would presumably oscillate short lines would be required to reach a +20% overshoot for this R_{dc} = 97.6Ω case. However, for short interconnects, even underdamped response characteristics may be useable if IC speeds are not very fast, as the absolute magnitudes of the interconnect delays are reduced. Note, however, that we have ignored the effects of load capacitance, C_L, here, and the simple $(R_{in} + R_{dc})C_L$ time constant effects can be severe for small normal metal lines.

In summary, these calculations of small normal metal lines response characteristics show that the assumptions for R_{MAX} made in the HTSC MCM/normal metal interconnect MCM tradeoff studies (References 5 and 6) were valid (just as the detailed "real world" netlist/wireability study of References 9 showed that our statistical wiring model assumptions were valid). These studies show that as the

number of die on MCMs increases, and particularly as the I/O counts on the die approach optimum values for MCM use (as opposed to I/O starved PCB-optimized ICs), it will become increasingly difficult to meet the requirements for MCM interconnects using normal metals. Although appropriate signal propagation has been shown to be practical at R_{dc} values as high as 25-50Ω, HTSC interconnects offering R_{dc} values far below the desired R_{MAX} = 10Ω range (even with ultra-high interconnect densities at linewidths of W = 2μm or so) should prove ideal for high performance, complex digital MCMs. Further, these HTSC interconnects should not show the signal anomalies due to complex, frequency dependent Z_o seem at the few percent level in small copper lines (eg. Figures 50, 1.17, etc.), which would make them attractive for mixed-mode (A/D) applications as well.

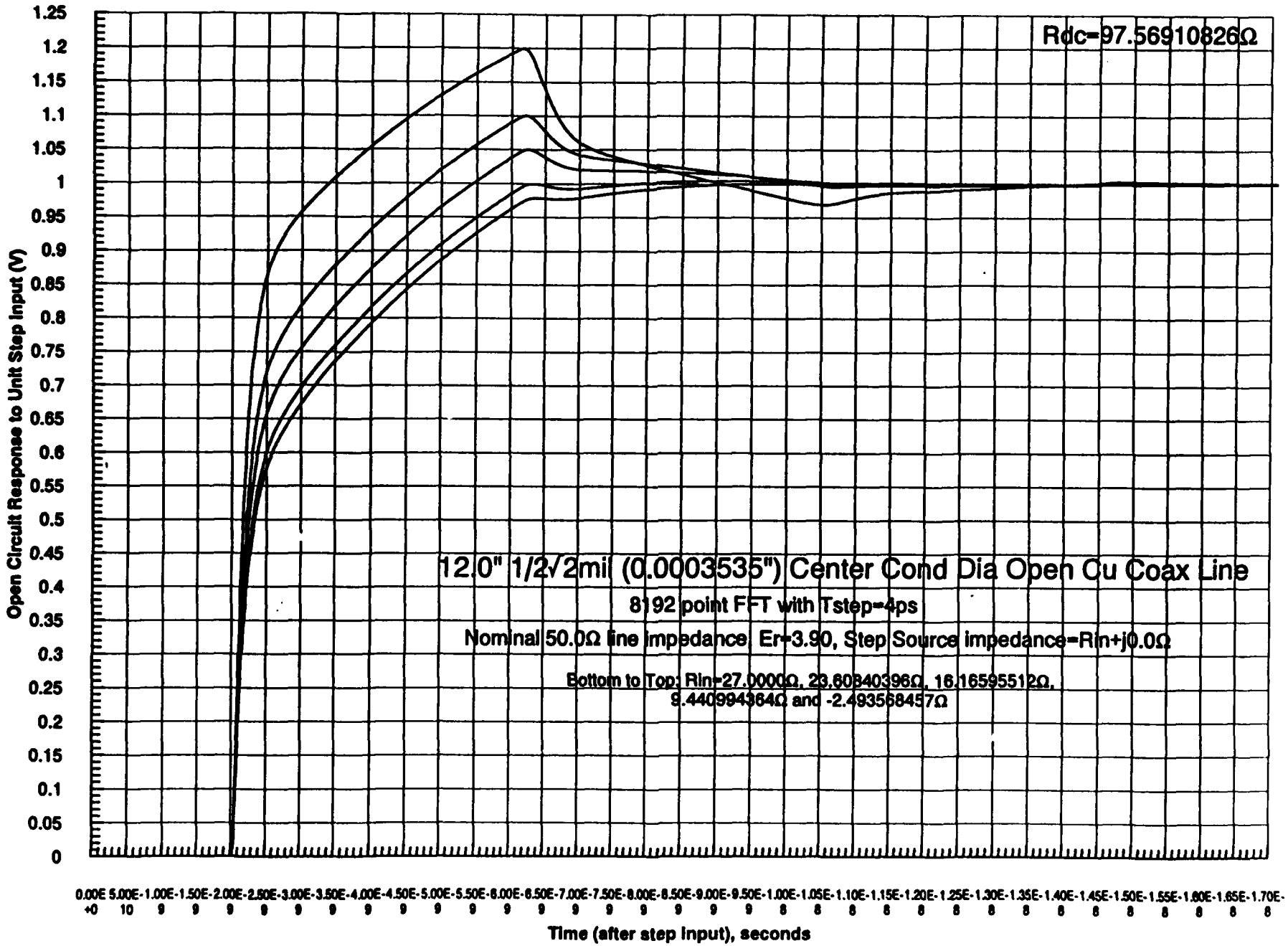

Rdc=97.56910826Ω
12.0" 1/2√2mil (0.0003535") Center Cond Dia Open Cu Coax Line
8192 point FFT with Tstep=4ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=27.0000Ω, 23.60340396Ω, 16.16595512Ω,
9.440994364Ω and -2.493568457Ω
Open Circuit Response to Unit Step Input (V)
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0.00E+0
5.00E-10
1.00E-9
1.50E-9
2.00E-9
2.50E-9
3.00E-9
3.50E-9
4.00E-9
4.50E-9
5.00E-9
5.50E-9
6.00E-9
6.50E-9
7.00E-9
7.50E-9
8.00E-9
8.50E-9
9.00E-9
9.50E-9
1.00E-8
1.05E-8
1.10E-8
1.15E-8
1.20E-8
1.25E-8
1.30E-8
1.35E-8
1.40E-8
1.45E-8
1.50E-8
1.55E-8
1.60E-8
1.65E-8
1.70E-8
Time (after step input), seconds

Figure 1.14

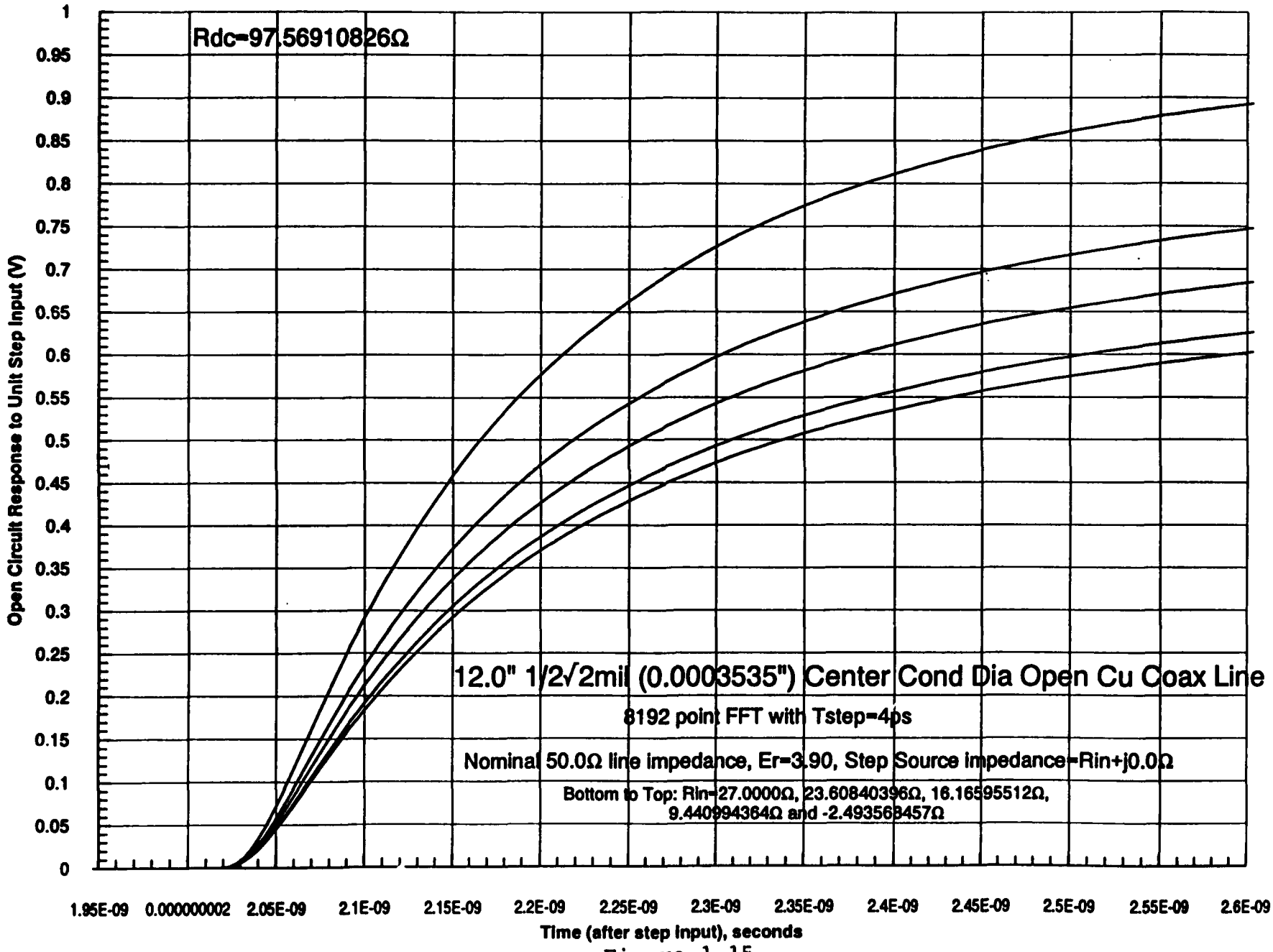

Rdc=97.569108260Ω
12.0" 1/2√2mil (0.0003535") Center Cond Dia Open Cu Coax Line
8192 point FFT with Tstep=4ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=27.0000Ω, 23.608403960Ω, 16.165955120Ω,
9.440994364Ω and -2.493568457Ω
Open Circuit Response to Unit Step Input (V)
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
1.95E-09
0.000000002
2.05E-09
2.1E-09
2.15E-09
2.2E-09
2.25E-09
2.3E-09
2.35E-09
2.4E-09
2.45E-09
2.5E-09
2.55E-09
2.6E-09
Time (after step input), seconds

Figure 1.15

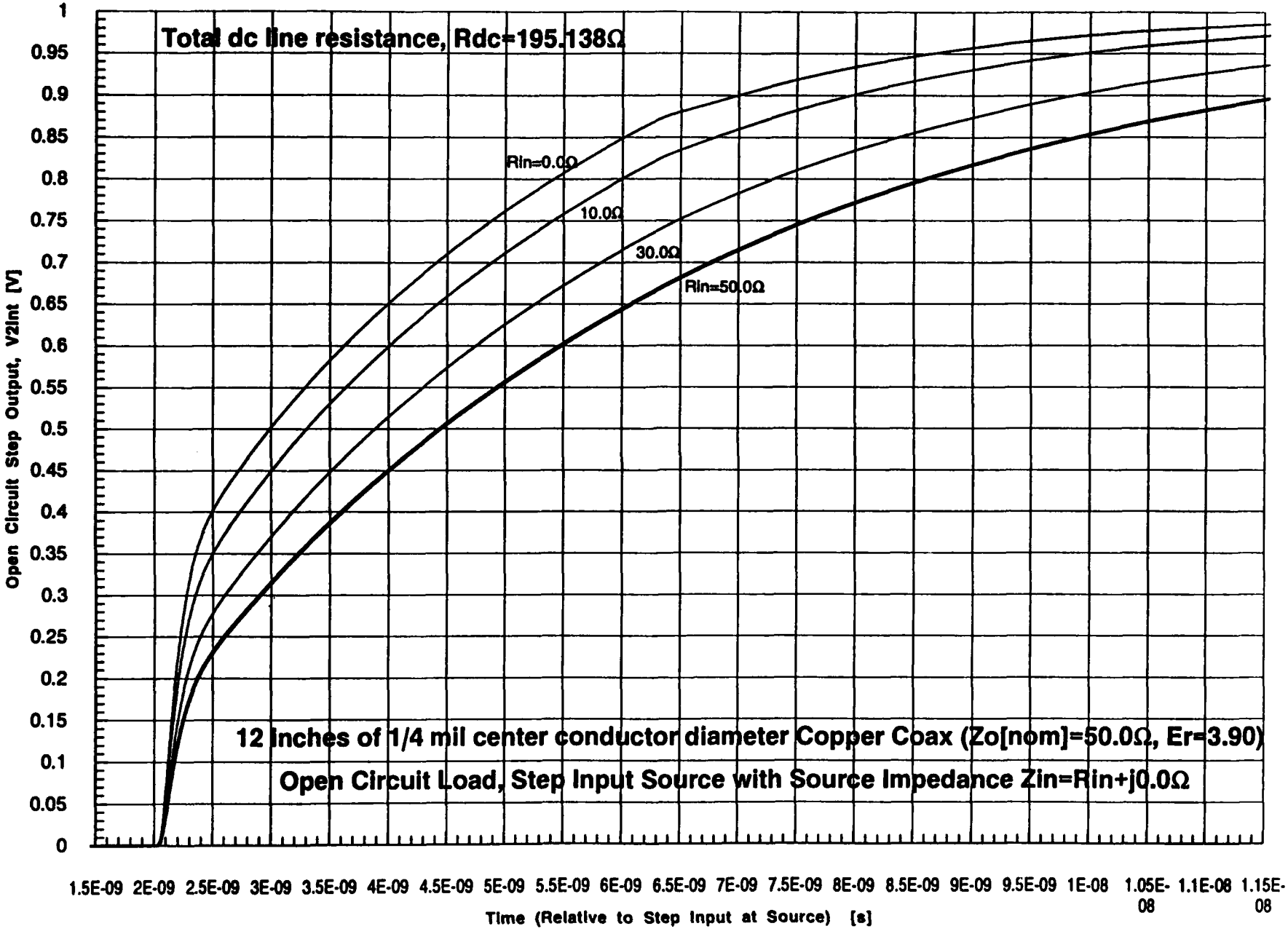

Total dc line resistance, Rdc=195.138Ω
Rin=0.0Ω
10.0Ω
30.0Ω
Rin=50.0Ω
12 inches of 1/4 mil center conductor diameter Copper Coax (Zo[nom]=50.0Ω, Er=3.90)
Open Circuit Load, Step Input Source with Source Impedance Zin=Rin+j0.0Ω
Open Circuit Step Output, V2int [V]
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
1.5E-09 2E-09 2.5E-09 3E-09 3.5E-09 4E-09 4.5E-09 5E-09 5.5E-09 6E-09 6.5E-09 7E-09 7.5E-09 8E-09 8.5E-09 9E-09 9.5E-09 1E-08 1.05E-08 1.1E-08 1.15E-08
Time (Relative to Step Input at Source) [s]

Figure 1.16

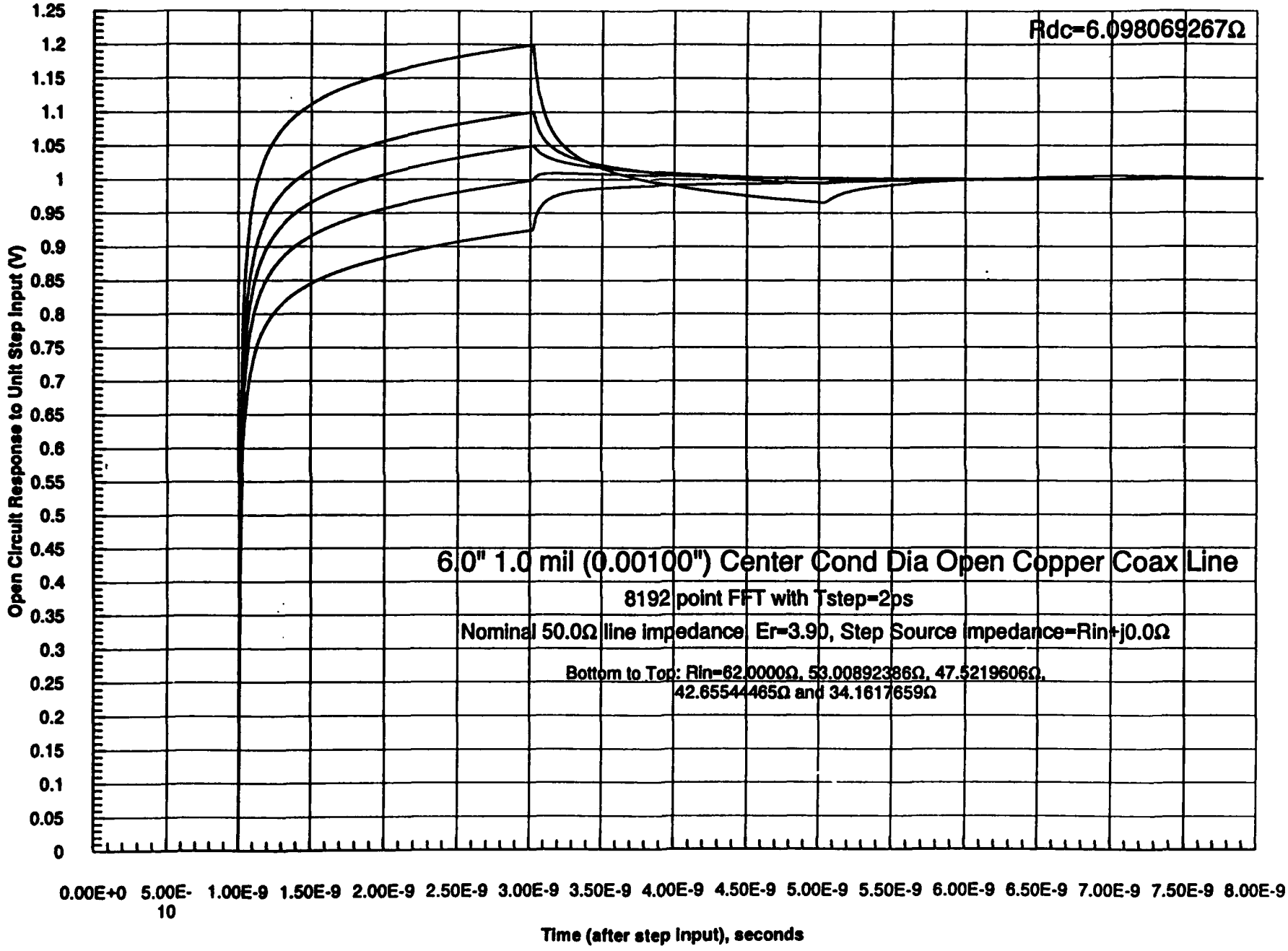

Rdc=6.098069267Ω
6.0" 1.0 mil (0.00100") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=2ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=62.0000Ω, 53.00892386Ω, 47.5219606Ω,
42.65544465Ω and 34.1617659Ω
Open Circuit Response to Unit Step Input (V)
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0.00E+0
5.00E-10
1.00E-9
1.50E-9
2.00E-9
2.50E-9
3.00E-9
3.50E-9
4.00E-9
4.50E-9
5.00E-9
5.50E-9
6.00E-9
6.50E-9
7.00E-9
7.50E-9
8.00E-9
Time (after step input), seconds

Figure 1.17

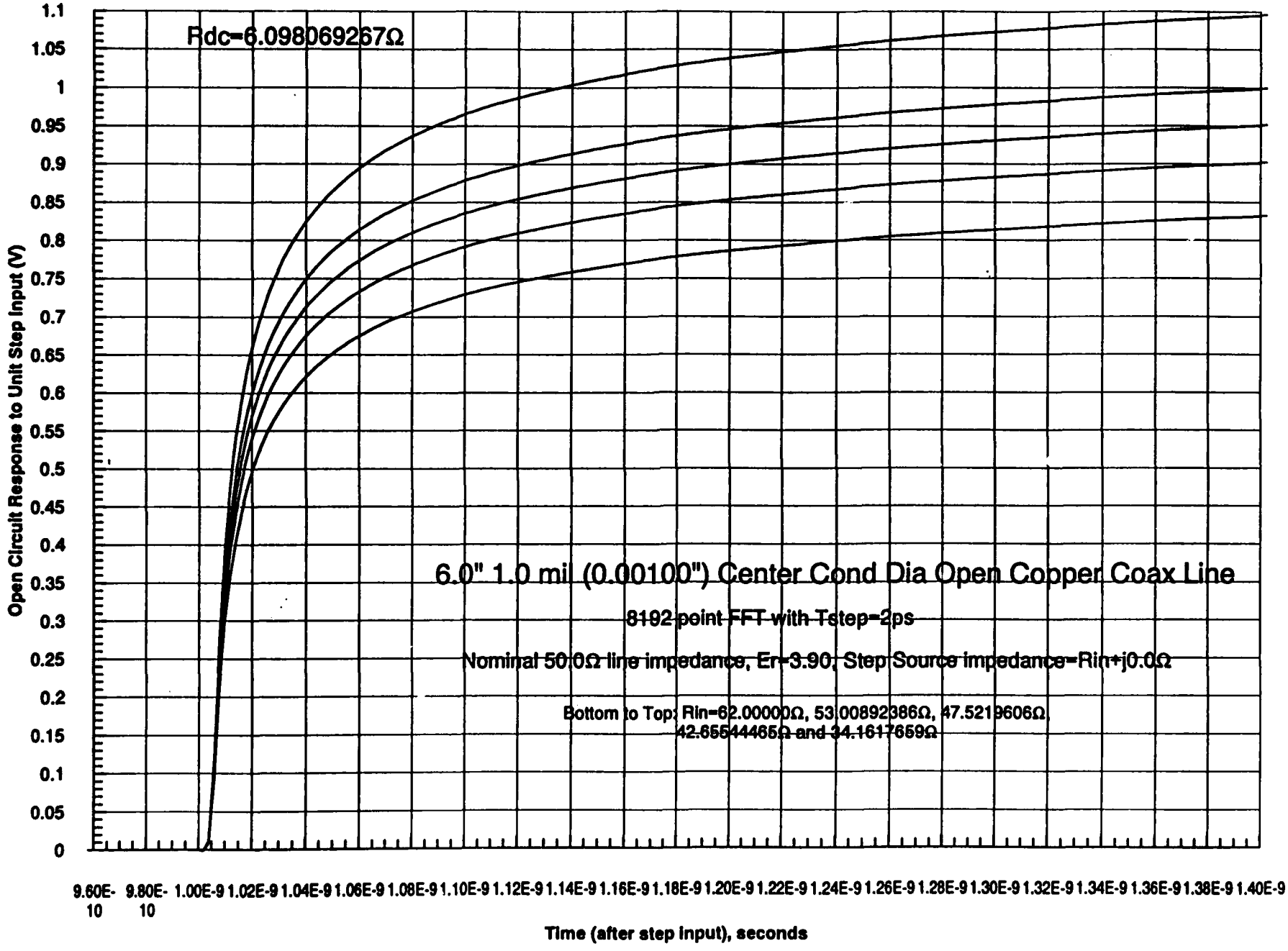

Rdc=6.098069267Ω
6.0" 1.0 mil (0.00100") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=2ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=62.00000Ω, 53.00892386Ω, 47.52196060Ω, 42.65544465Ω and 34.16176590Ω
Open Circuit Response to Unit Step Input (V)
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
9.60E-10
9.80E-10
1.00E-9
1.02E-9
1.04E-9
1.06E-9
1.08E-9
1.10E-9
1.12E-9
1.14E-9
1.16E-9
1.18E-9
1.20E-9
1.22E-9
1.24E-9
1.26E-9
1.28E-9
1.30E-9
1.32E-9
1.34E-9
1.36E-9
1.38E-9
1.40E-9
Time (after step input), seconds

Figure 1.18

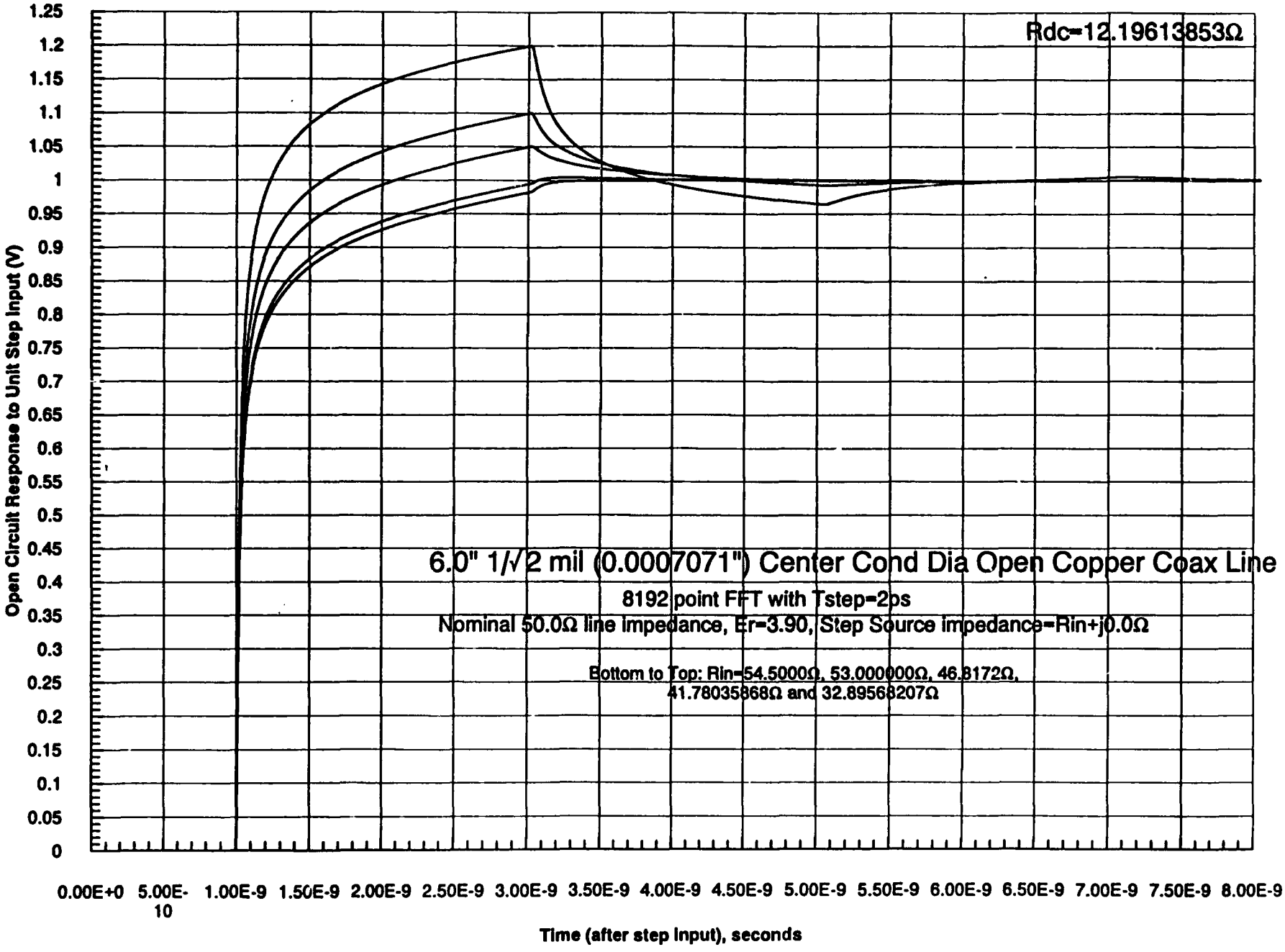

Rdc=12.19613853Ω
6.0" 1/√2 mil (0.0007071") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=2ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=54.5000Ω, 53.000000Ω, 46.8172Ω,
41.78035868Ω and 32.89568207Ω
Open Circuit Response to Unit Step Input (V)
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0.00E+0
5.00E-10
1.00E-9
1.50E-9
2.00E-9
2.50E-9
3.00E-9
3.50E-9
4.00E-9
4.50E-9
5.00E-9
5.50E-9
6.00E-9
6.50E-9
7.00E-9
7.50E-9
8.00E-9
Time (after step input), seconds

Figure 1.19

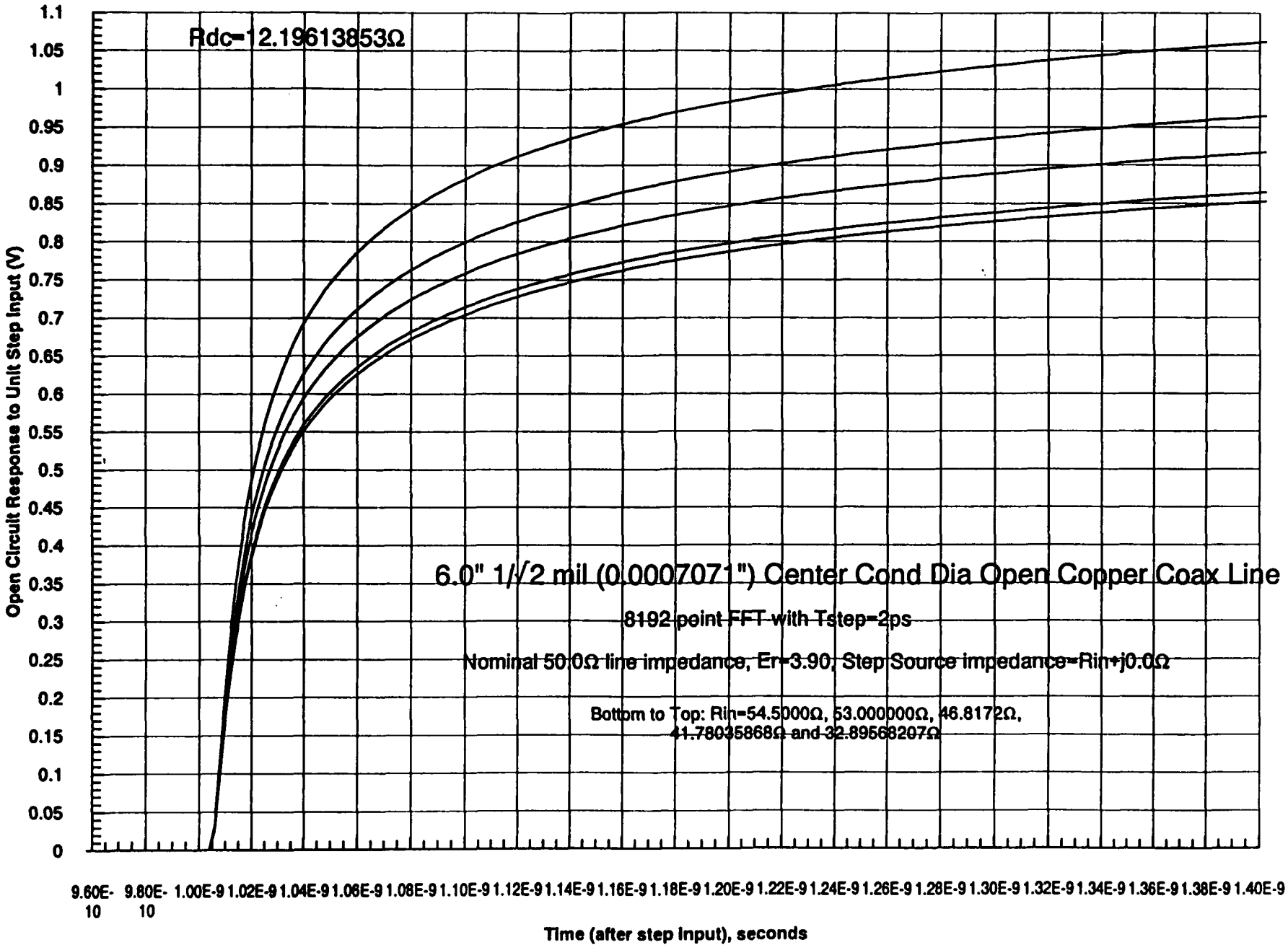

Rdc=12.19613853Ω
6.0" 1/√2 mil (0.0007071") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=2ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=54.5000Ω, 53.000000Ω, 46.8172Ω,
41.78035868Ω and 32.89568207Ω
Open Circuit Response to Unit Step Input (V)
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
9.60E-10
9.80E-10
1.00E-9
1.02E-9
1.04E-9
1.06E-9
1.08E-9
1.10E-9
1.12E-9
1.14E-9
1.16E-9
1.18E-9
1.20E-9
1.22E-9
1.24E-9
1.26E-9
1.28E-9
1.30E-9
1.32E-9
1.34E-9
1.36E-9
1.38E-9
1.40E-9
Time (after step input), seconds

Figure 1.20

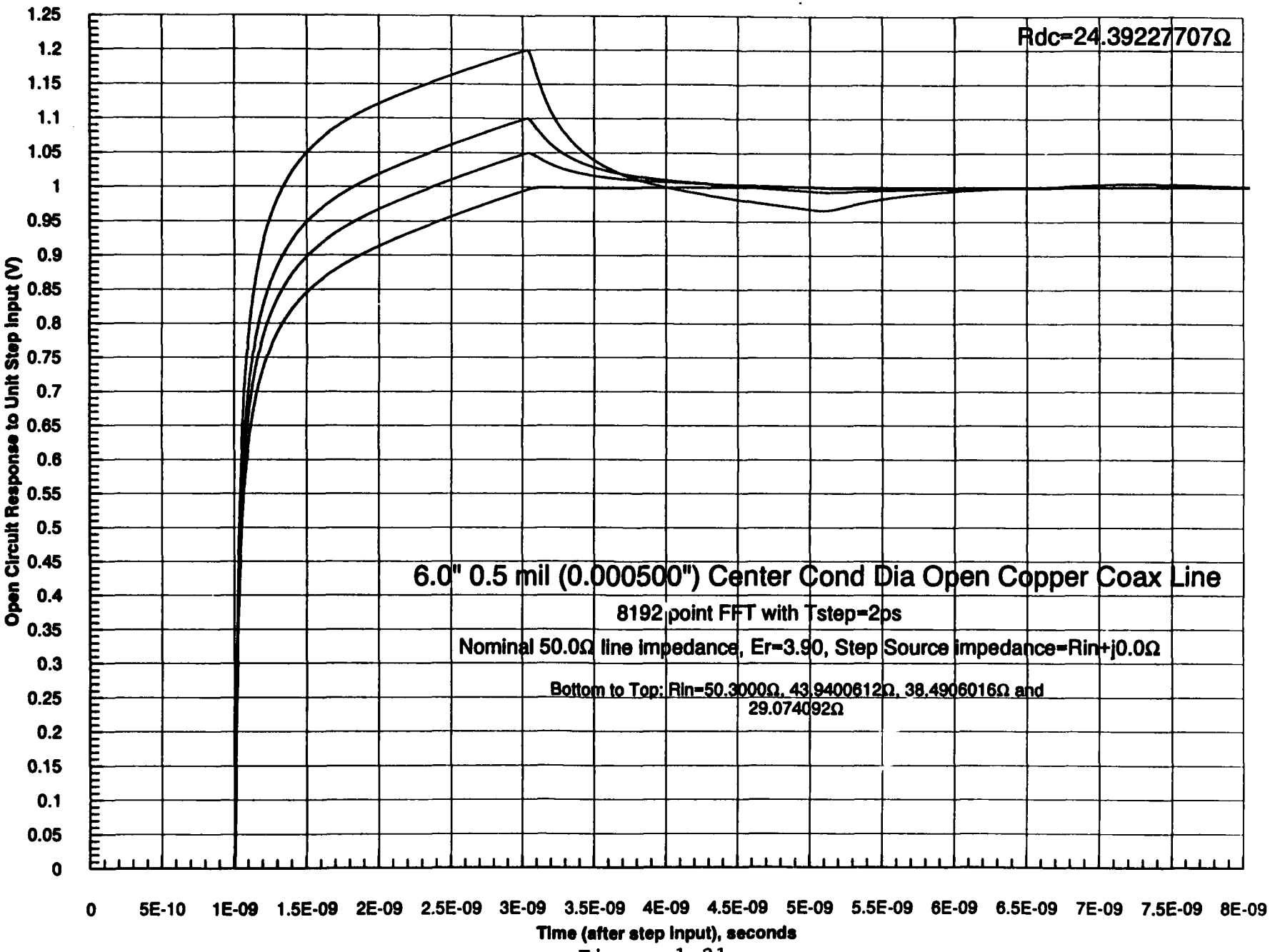

Rdc=24.39227707Ω
6.0" 0.5 mil (0.000500") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=2ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=50.3000Ω, 43.9400612Ω, 38.4906016Ω and 29.074092Ω
Open Circuit Response to Unit Step Input (V)
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0
5E-10
1E-09
1.5E-09
2E-09
2.5E-09
3E-09
3.5E-09
4E-09
4.5E-09
5E-09
5.5E-09
6E-09
6.5E-09
7E-09
7.5E-09
8E-09
Time (after step input), seconds

Figure 1.21

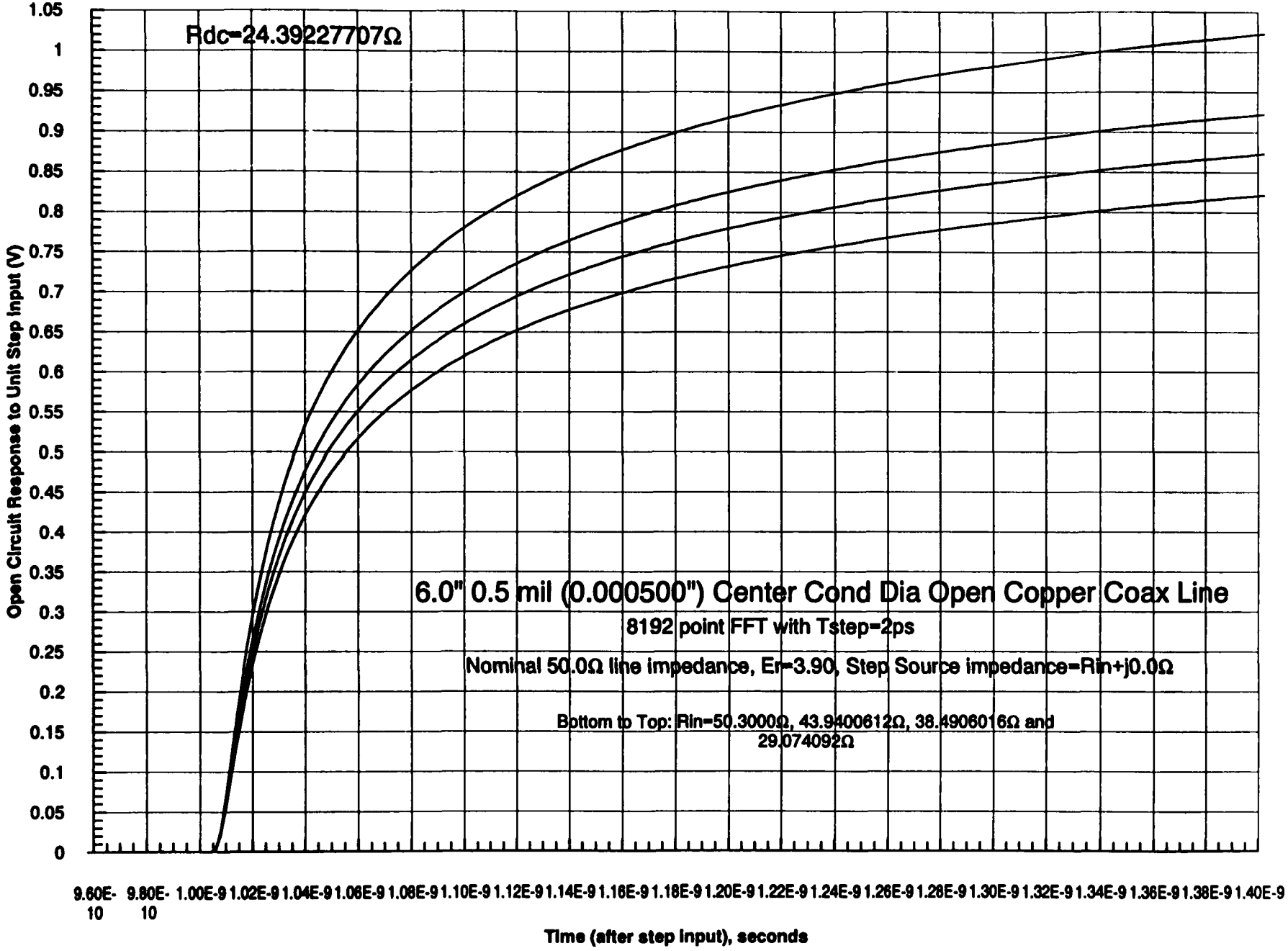

Rdc=24.39227707Ω
6.0" 0.5 mil (0.000500") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=2ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=50.3000Ω, 43.9400612Ω, 38.4906016Ω and 29.074092Ω
Open Circuit Response to Unit Step Input (V)
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
9.60E-10
9.80E-10
1.00E-9
1.02E-9
1.04E-9
1.06E-9
1.08E-9
1.10E-9
1.12E-9
1.14E-9
1.16E-9
1.18E-9
1.20E-9
1.22E-9
1.24E-9
1.26E-9
1.28E-9
1.30E-9
1.32E-9
1.34E-9
1.36E-9
1.38E-9
1.40E-9
Time (after step input), seconds

Figure 1.22

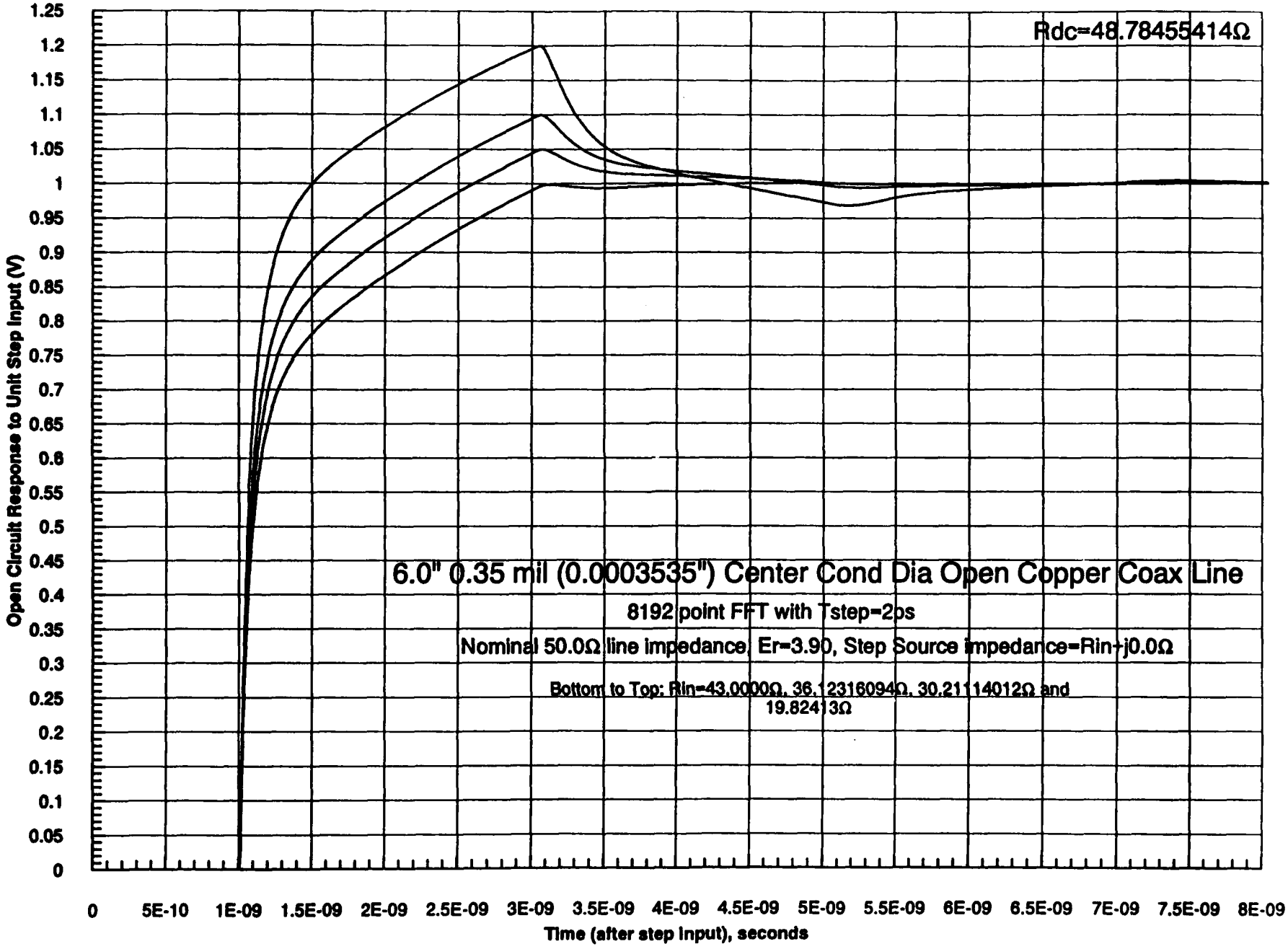

Rdc=48.78455414Ω
6.0" 0.35 mil (0.0003535") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=2ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=43.0000Ω, 36.12316094Ω, 30.21114012Ω and 19.82413Ω
Open Circuit Response to Unit Step Input (V)
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0
5E-10
1E-09
1.5E-09
2E-09
2.5E-09
3E-09
3.5E-09
4E-09
4.5E-09
5E-09
5.5E-09
6E-09
6.5E-09
7E-09
7.5E-09
8E-09
Time (after step input), seconds

Figure 1.23

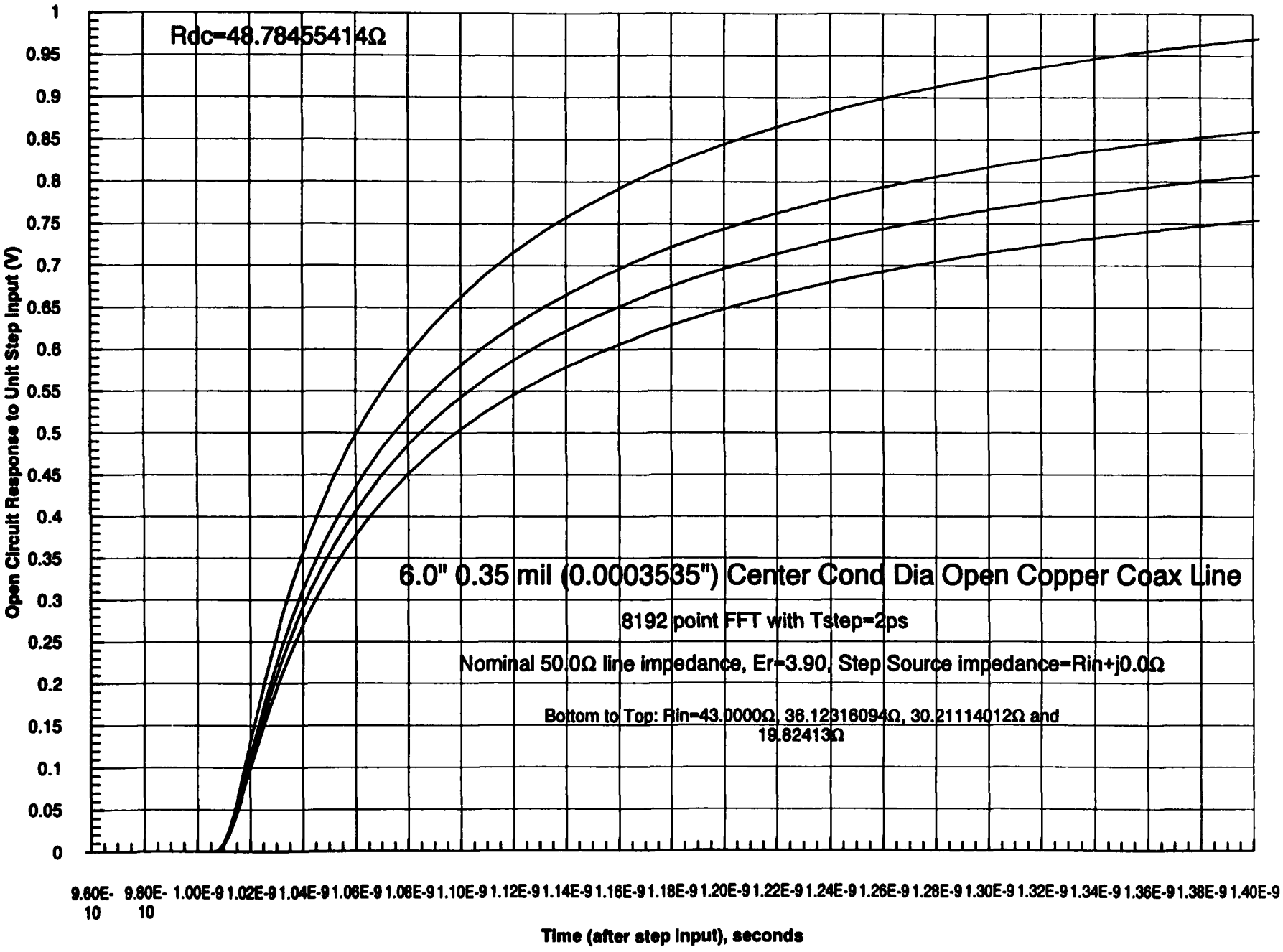

Rdc=48.784554140Ω
6.0" 0.35 mil (0.0003535") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=2ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=43.0000Ω, 36.12316094Ω, 30.21114012Ω and 19.82413Ω
Open Circuit Response to Unit Step Input (V)
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
9.60E-10
9.80E-10
1.00E-9
1.02E-9
1.04E-9
1.06E-9
1.08E-9
1.10E-9
1.12E-9
1.14E-9
1.16E-9
1.18E-9
1.20E-9
1.22E-9
1.24E-9
1.26E-9
1.28E-9
1.30E-9
1.32E-9
1.34E-9
1.36E-9
1.38E-9
1.40E-9
Time (after step input), seconds

Figure 1.24

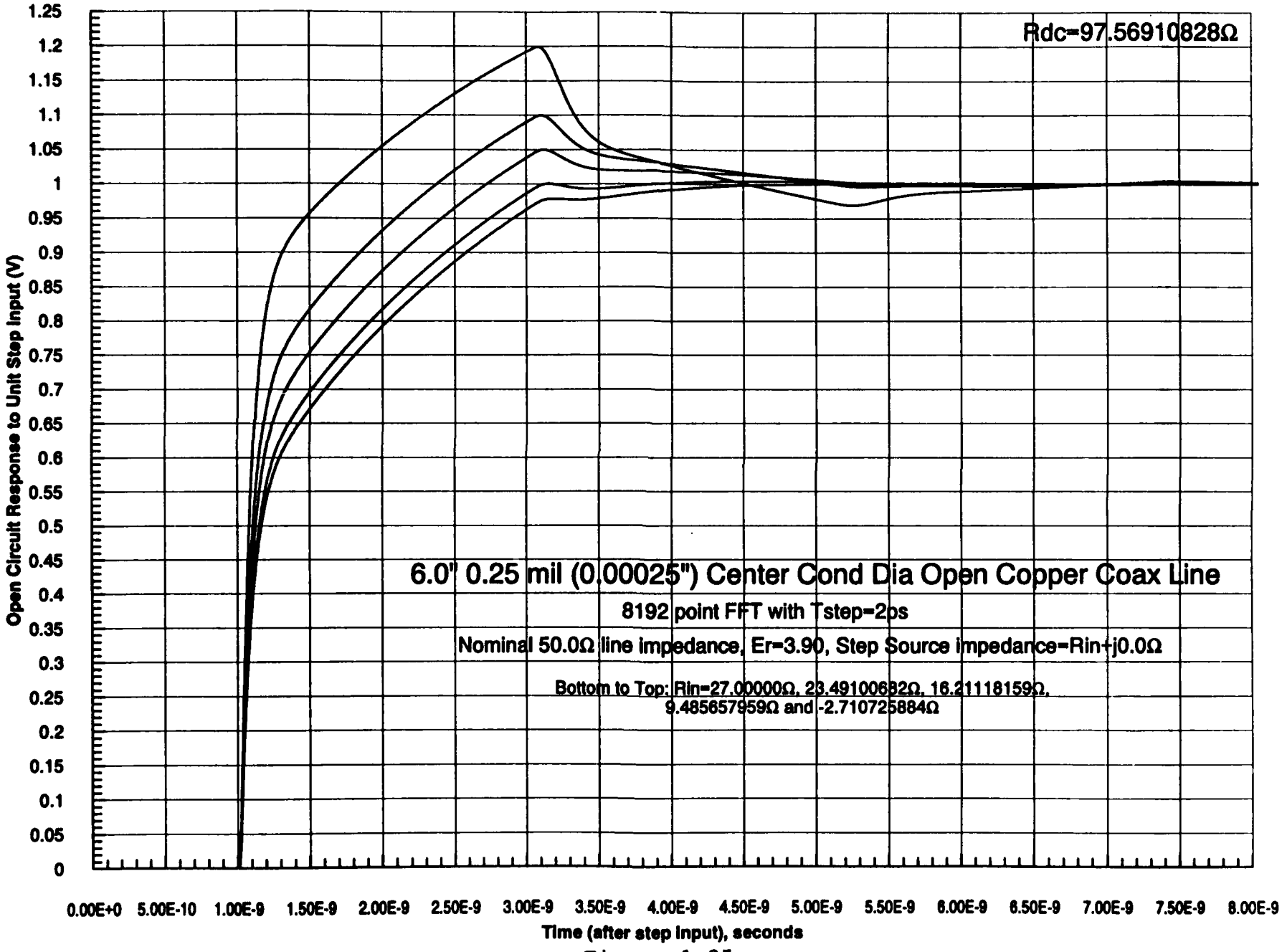

Rdc=97.56910828Ω
6.0" 0.25 mil (0.00025") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=2ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=27.00000Ω, 23.49100682Ω, 16.21118159Ω,
9.485657959Ω and -2.710725884Ω
Open Circuit Response to Unit Step Input (V)
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0.00E+0
5.00E-10
1.00E-9
1.50E-9
2.00E-9
2.50E-9
3.00E-9
3.50E-9
4.00E-9
4.50E-9
5.00E-9
5.50E-9
6.00E-9
6.50E-9
7.00E-9
7.50E-9
8.00E-9
Time (after step input), seconds

Figure 1.25

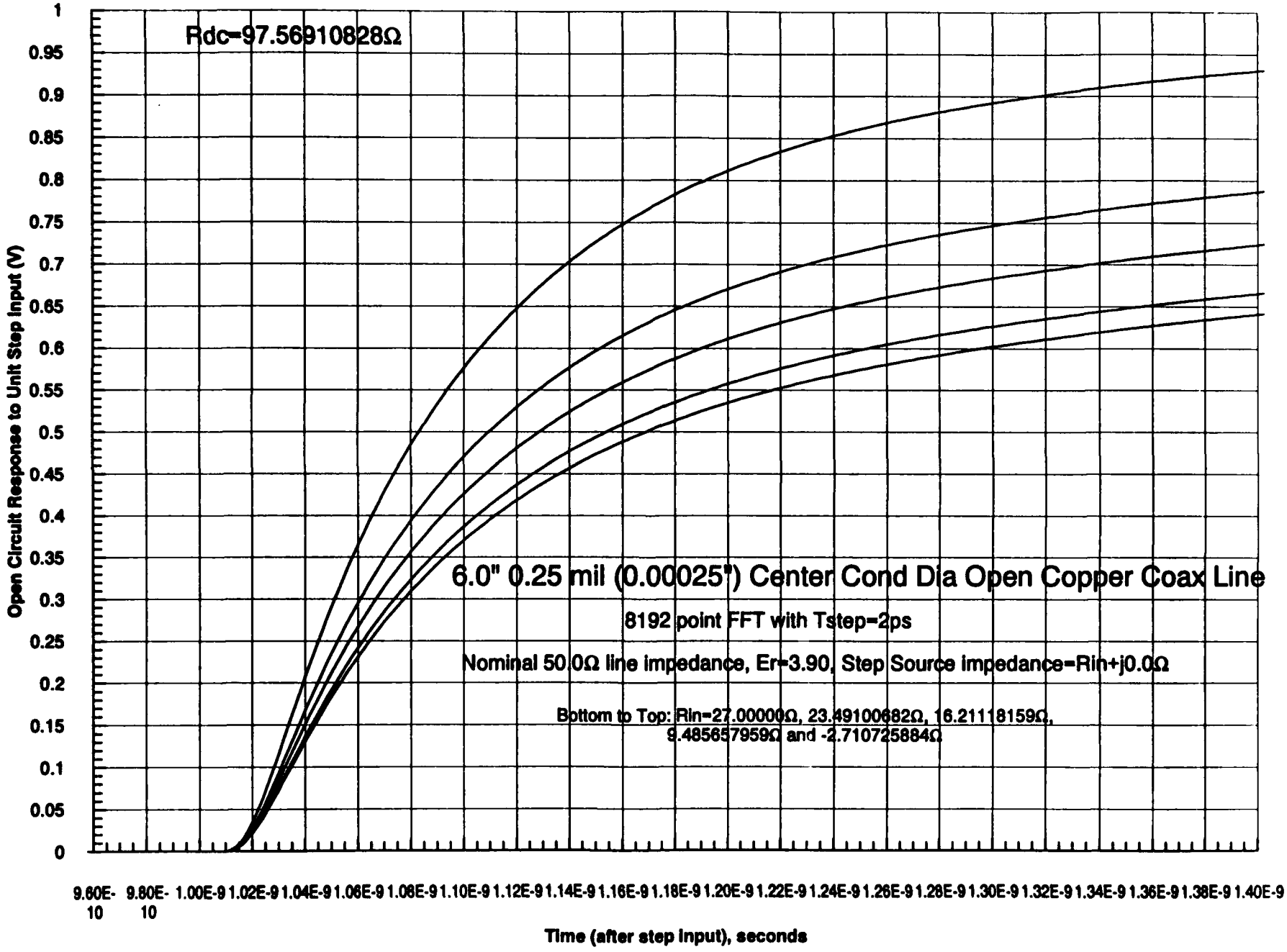

Rdc=97.56910828Ω
6.0" 0.25 mil (0.00025") Center Cond Dia Open Copper Coax Line
8192 point FFT with Tstep=2ps
Nominal 50.0Ω line impedance, Er=3.90, Step Source impedance=Rin+j0.0Ω
Bottom to Top: Rin=27.00000Ω, 23.49100682Ω, 16.21118159Ω,
9.4856579590 and -2.7107258840
Open Circuit Response to Unit Step Input (V)
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
9.60E-10
9.80E-10
1.00E-9
1.02E-9
1.04E-9
1.06E-9
1.08E-9
1.10E-9
1.12E-9
1.14E-9
1.16E-9
1.18E-9
1.20E-9
1.22E-9
1.24E-9
1.26E-9
1.28E-9
1.30E-9
1.32E-9
1.34E-9
1.36E-9
1.38E-9
1.40E-9
Time (after step input), seconds

Figure 1.26

References

1. Ramo, Whinnery and Van Duyer, "Fields and Waves in Communications Electronics", John Wiley & Sons, New York 1965, pp. 249-252, 286-293 and 444-446.

2. Fred E. Gardiol, "Lossy Transmission Lines," Artech House, Inc., 1987.

3. Lawrence M. Rubin, "CAE Tools for Veryfying High Performance Digital Systems", Proceedings of SPIE/OPCON 90 Microelectronic Interconects and Packaging: System and Process Integration Vol 1390, pp. 336-358, 1990.

4. Richard B. Alder, Lan Jen Chu, and Robert M. Fano, "Electromagnetic Energy Transmission and Radiation," John Wiley and Sons, 1959.

5. "Applicability of Superconducting Interconnection Technology for High Speed ICs and Systems", Final Report on DARPA BAA 90-06 Contract N00014-90-C-0217, October 1991.

6. SBIR Final report, "High Density Multi-Layer Interconnects for High Speed Digital MCMs", DARPA BAA 90-114, Contract DAAG01-91-C-R038, December 1991.

7. "Reference Data for Engineers: Radio, Electronics, Computer and Communications - Seventh Edition", Edward C. Jordan, SAMS, Carmel, Indiana, ISBN 0-672-21563-2, Chapter 29, pp. 29-1 to 29-7.

8. Abramowite and Stegun, "Handbook of Mathematical Functions", National Bureau of Standards Applied Mathematics Series 55, US Government Printing Office, Wash. DC, Sections 9.9-9.11 and Table 9.12.

9. SBIR Final Report, "Application of HTSC Interconnects for High Speed Digtial Electronic Circuitry", DARPA DAA 91-076, Contract DAAH01-91-C-R185, December 1992.

SECTION 2

Q3 1992
QUARTERLY REPORT

Q3 1992 Quarterly

2.1. Transit Response Characteristics of Small MCM Interconnect Lines

2.1.1. Background

The report is a continuation of work presented in the previous two quarterly reports and will continue numbering equations, references, and figures from where they left off. For reference, Equations 1-24 were in the March 1992 Quarterly Report, along with References 1-4 and Figures 1-15. Equations 25-45 are in the June 1992 Quarterly Report, along with References 5-8 and Figures 16-35. Hence the equations in this report begin with Equation 47 and the figures begin with Figure 36.

Described in the previous report was the development of a highly accurate Fourier transform method of determining the transient response of small lossy lines. The key to this analysis is the use of both the complex propagation constant and the complex frequency-dependent characteristic impedance of the small diameter lines (eg. center conductor diameters from 0.25 and to 1 mil in small copper coax lines have been analyzed). The principal focus of this report will be on presenting extensive data on many different simulation runs of this program. However, as a reference point for the analyses, it is important to review briefly what lossless (ideal) transmission lines behave like under similar circumstances.

2.1.2. Lossless Transmission Line Transient Response

Consider the classical source terminated, open-load transmission line configuration shown in Figure 36. When a voltage step of magnitude V_{in} is applied at $t = 0$ through a source resistance, R_{in}, to the input end of a lossless ($R_{dc} = 0$) line, for a period of time of $2\tau_{pd}$ (before current reflections from the load end of the line arrive back at the source end), the line input voltage, V_1, is given by

$$V_1 = \frac{V_{in} Z_o}{R_{in} + Z_o} \quad \text{for } 0 < t < \tau_{pd} \qquad \text{Eq. 47}$$

The voltage reflection coefficient at the end of the line is given by (eg. Reference 7)

$$\rho = \frac{Z_2 - Z_o}{Z_2 + Z_o} \qquad \text{Eq. 48}$$

For this open-circuit case, $Z_2 = \infty$ and $\rho = +1$, which means that the load voltage,V_2 will be twice the voltages on the line, so that the initial output voltage step is

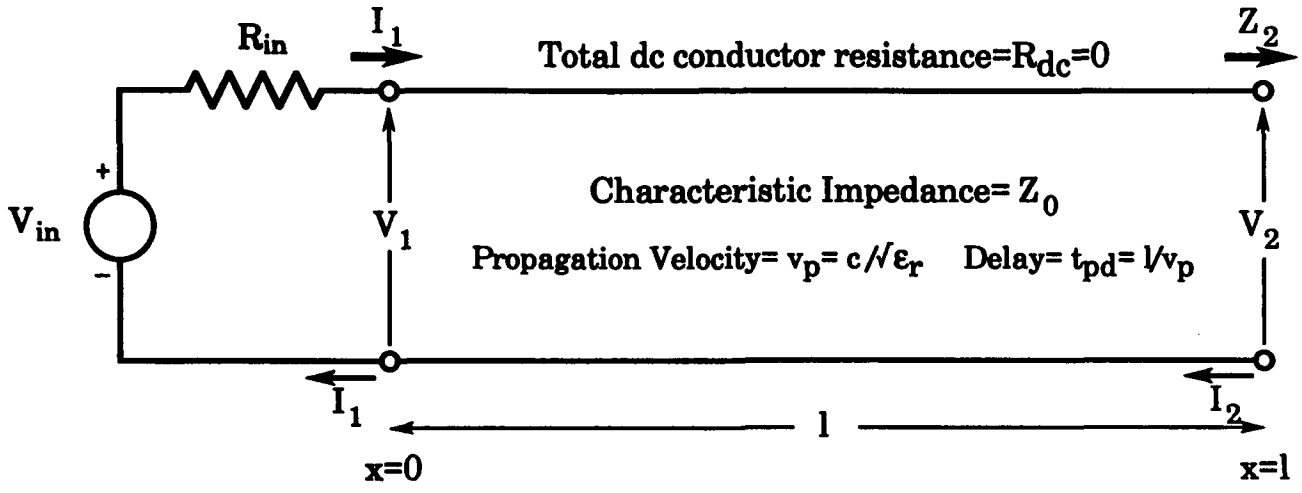
$$V_2 = \frac{2 V_{in} Z_o}{R_{in} + Z_o} \quad \text{for } \tau_{pd} < t < 3\tau_{pd} \qquad \text{Eq. 49}$$

Defining the initial voltage overshoot for this lossless line case as

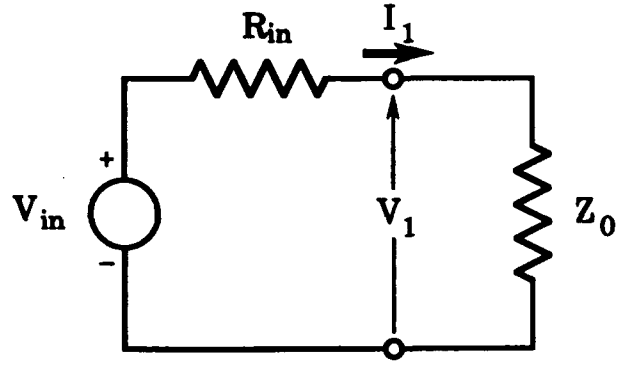
$$\text{Overshoot} = \frac{V_2 - V_{in}}{V_{in}} \quad \text{for } \tau_{pd} < t < 3\tau_{pd} \qquad \text{Eq. 50}$$

we can plot the expected overshoot versus source resistance for this lossless line case. This is shown for $Z_o = 50\Omega$ in Figure 37 over a wide range of generator resistances (log scale for $1\Omega \le R_{in} \le 10{,}000\Omega$), and in more detail for R_{in} near Z_o in Figure 38. These curves are very handy, for example, for investigating the use of

Lossless Transmission Line



Model for initial pulse response at the input for $0<t<2t_{pd}$ (before I_2 reflections arrive back at input):



$$V_1 = \frac{V_{in} Z_0}{R_{in} + Z_0}$$

$$I_1 = \frac{V_{in}}{R_{in} + Z_0}$$

Figure 36

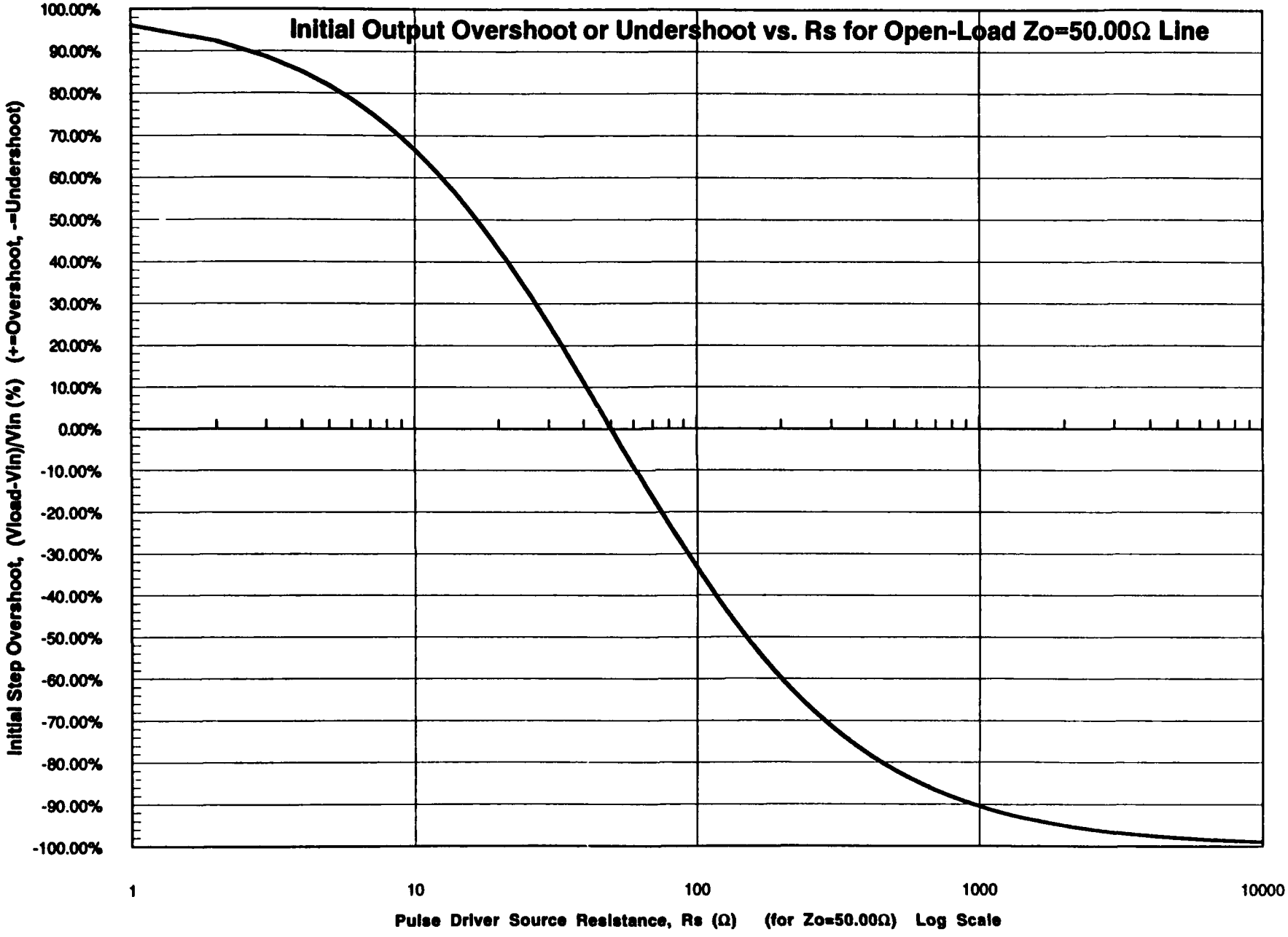

Initial Output Overshoot or Undershoot vs. Rs for Open-Load Zo=50.00Ω Line
Initial Step Overshoot, (Vload-Vin)/Vin (%) (+=Overshoot, -=Undershoot)
100.00%
90.00%
80.00%
70.00%
60.00%
50.00%
40.00%
30.00%
20.00%
10.00%
0.00%
-10.00%
-20.00%
-30.00%
-40.00%
-50.00%
-60.00%
-70.00%
-80.00%
-90.00%
-100.00%
1
10
100
1000
10000
Pulse Driver Source Resistance, Rs (Ω) (for Zo=50.00Ω) Log Scale

Figure 37

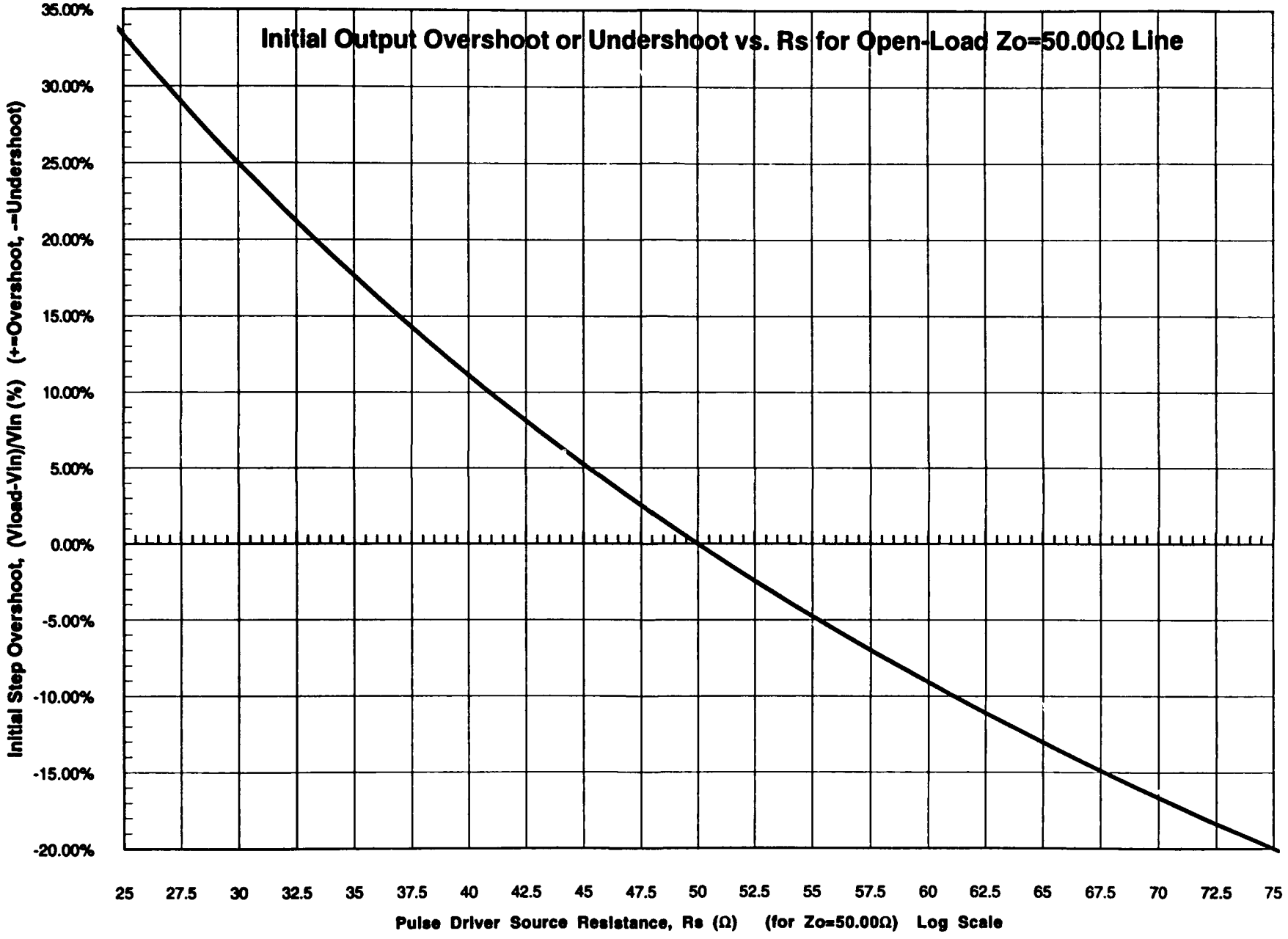

Initial Output Overshoot or Undershoot vs. Rs for Open-Load Zo=50.00Ω Line
Initial Step Overshoot, (Vload-Vin)/Vin (%) (+=Overshoot, -=Undershoot)
35.00%
30.00%
25.00%
20.00%
15.00%
10.00%
5.00%
0.00%
-5.00%
-10.00%
-15.00%
-20.00%
25 27.5 30 32.5 35 37.5 40 42.5 45 47.5 50 52.5 55 57.5 60 62.5 65 67.5 70 72.5 75
Pulse Driver Source Resistance, Rs (Ω) (for Zo=50.00Ω) Log Scale

Figure 38

self-terminating lines (these are lossy lines where the R_{dc} of the line is compensated for by reducing R_{in} below Z_o). The problem with this is that if the longest lines are properly compensated by reducing R_{in} from 50Ω to 25Ω, for example, then shorter lines (which have small series resistance and hence are nearly lossless) can give excessive overshoot (eg. 33.3% for R_{in} = 25Ω in Figure 38). Not only can this overshoot itself cause problems with IC inputs, but large overshoots are accompanied by a substantial undershoot, given by

$$V_2 = 4\,V_{in}\frac{R_{in}\,Z_o}{\left(R_{in}+Z_o\right)^2} \quad \text{for } 3\,\tau_{pd} < t < 5\,\tau_{pd} \qquad \text{Eq. 51}$$

This can seriously compromise noise margin if the overshoot is serious. Of course, the same is true of undershoot in the output pulse waveform, which occurs for $R_{in} > Z_o$ in lossless lines.

Figures 39 through 49 illustrate these overshoot and undershoot characteristics for lossless lines, as a helpful reference point for both design purposes and for interpreting the detailed lossy line computer analysis results in Section 2.3. The generator resistances, R_{in} (called R_s in these particular figures), have been selected in this sequence of figures to give overshoot values of +50%, +40%, +30%, +20%, +10%, +5%, +0%, and -5% (5% undershoot), -10%, -20%, and -50%.

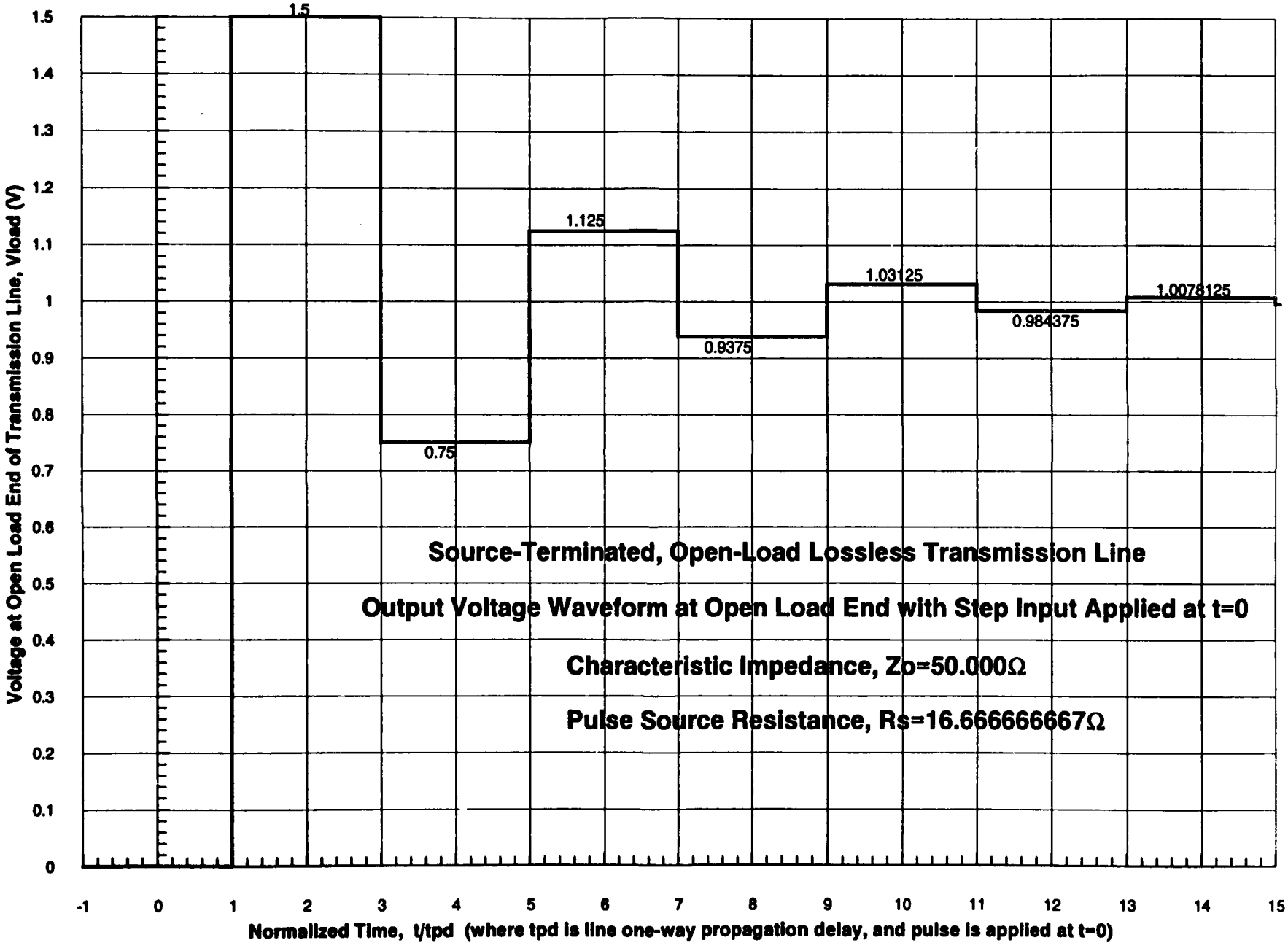

1.5
1.125
1.03125
1.0078125
0.984375
0.9375
0.75
Source-Terminated, Open-Load Lossless Transmission Line
Output Voltage Waveform at Open Load End with Step Input Applied at t=0
Characteristic Impedance, Zo=50.000Ω
Pulse Source Resistance, Rs=16.666666667Ω
Voltage at Open Load End of Transmission Line, Vload (V)
Normalized Time, t/tpd (where tpd is line one-way propagation delay, and pulse is applied at t=0)

Figure 39

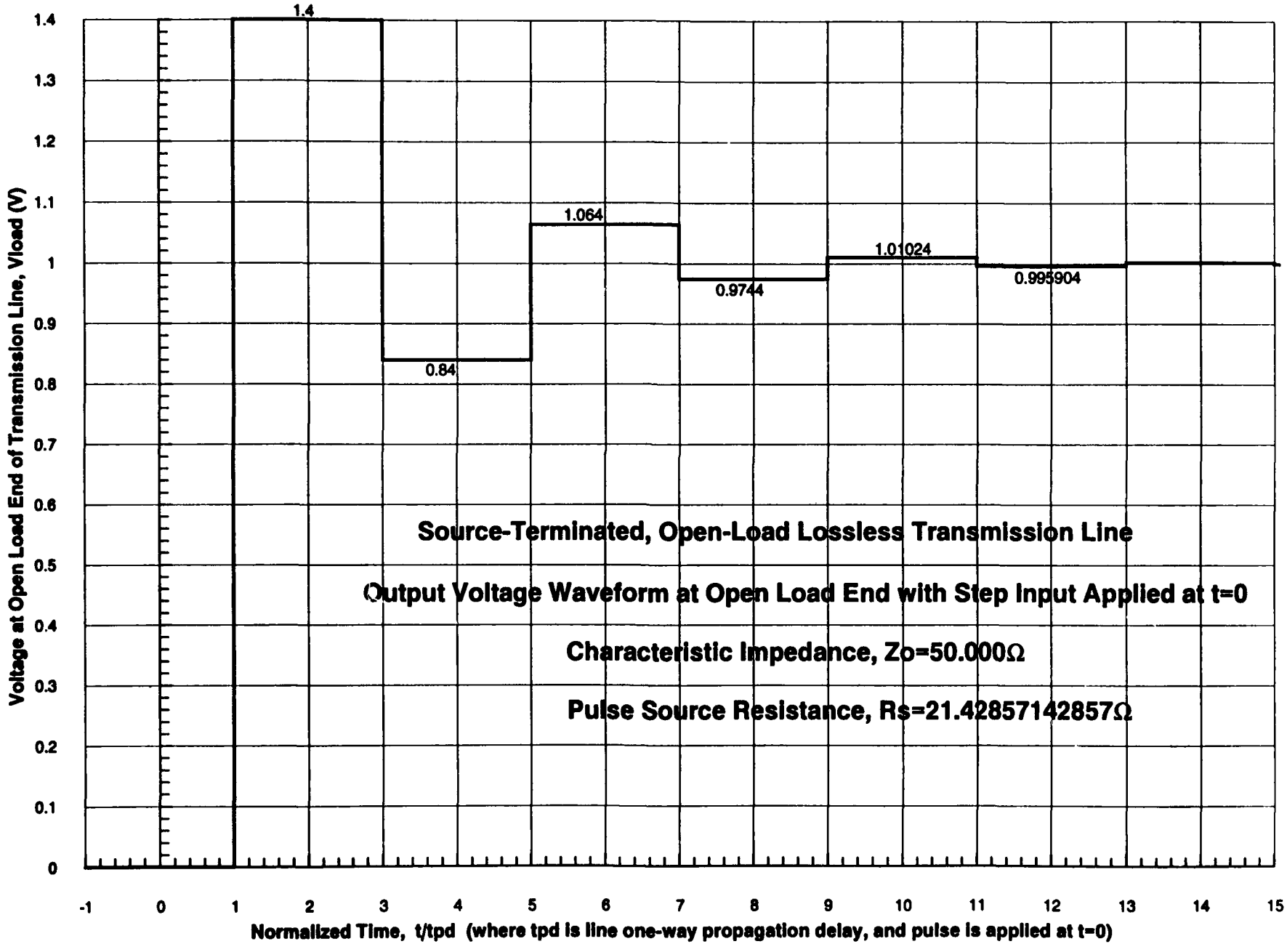

1.4
1.064
1.01024
0.9744
0.995904
0.84
Source-Terminated, Open-Load Lossless Transmission Line
Output Voltage Waveform at Open Load End with Step Input Applied at t=0
Characteristic Impedance, Zo=50.000Ω
Pulse Source Resistance, Rs=21.42857142857Ω
Voltage at Open Load End of Transmission Line, Vload (V)
Normalized Time, t/tpd (where tpd is line one-way propagation delay, and pulse is applied at t=0)
1.4
1.3
1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Figure 40

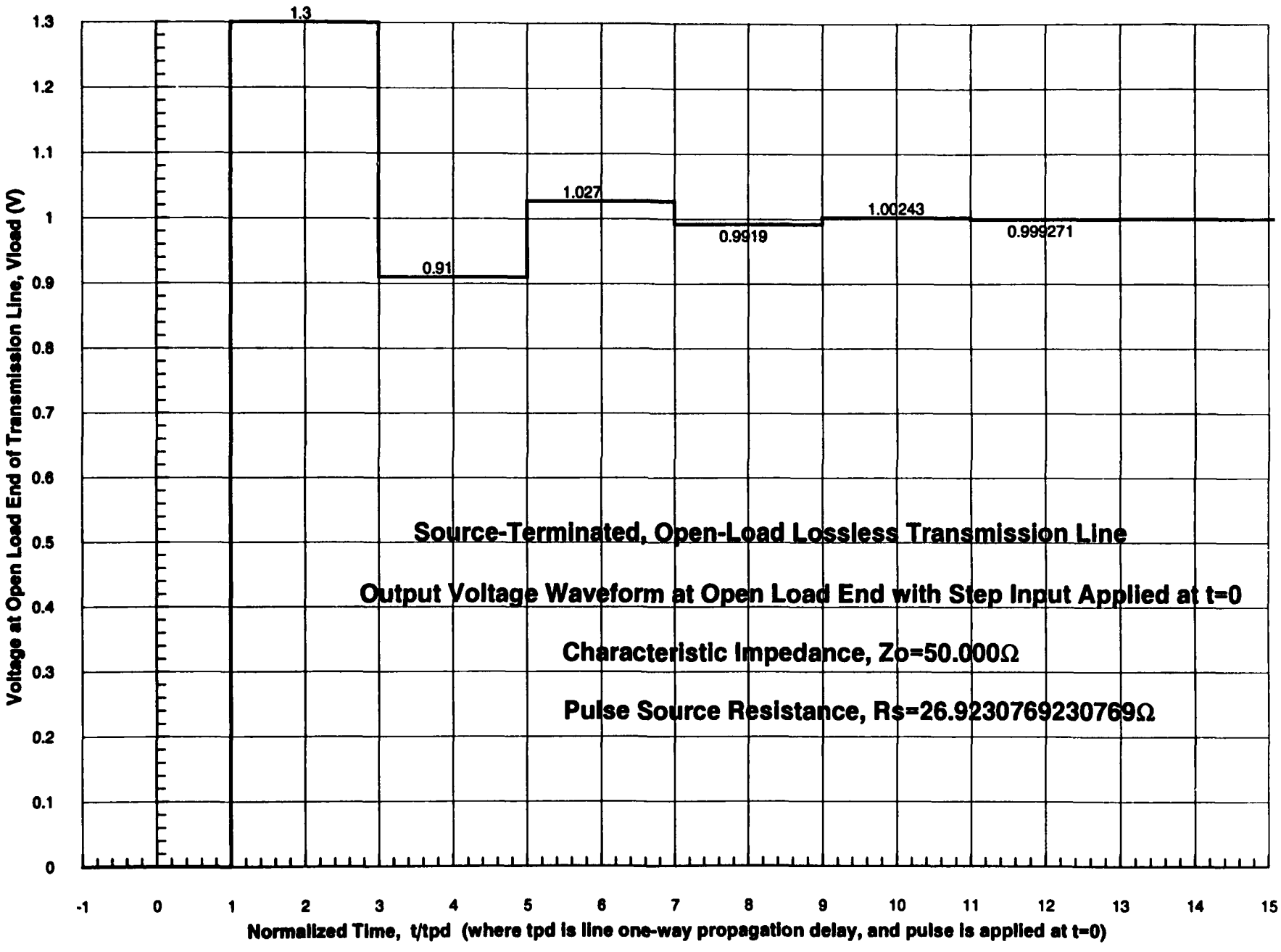

1.3
0.91
1.027
0.9919
1.00243
0.999271
Source-Terminated, Open-Load Lossless Transmission Line
Output Voltage Waveform at Open Load End with Step Input Applied at t=0
Characteristic Impedance, Zo=50.000Ω
Pulse Source Resistance, Rs=26.9230769230769Ω
Voltage at Open Load End of Transmission Line, Vload (V)
Normalized Time, t/tpd (where tpd is line one-way propagation delay, and pulse is applied at t=0)
1.3
1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Figure 41

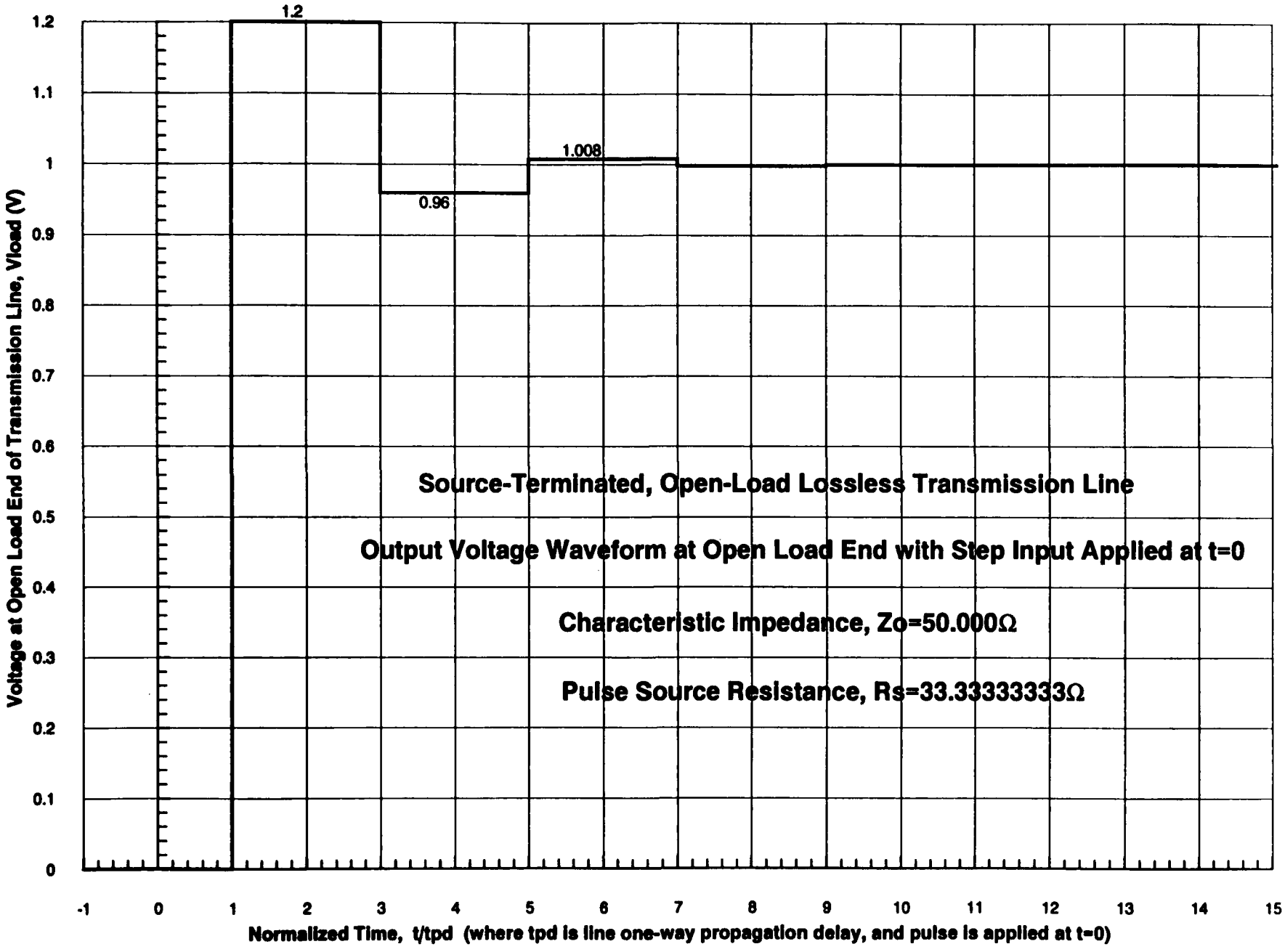

1.2
1.008
0.96
Source-Terminated, Open-Load Lossless Transmission Line
Output Voltage Waveform at Open Load End with Step Input Applied at t=0
Characteristic Impedance, Zo=50.000Ω
Pulse Source Resistance, Rs=33.33333333Ω
Voltage at Open Load End of Transmission Line, Vload (V)
Normalized Time, t/tpd (where tpd is line one-way propagation delay, and pulse is applied at t=0)
1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Figure 42

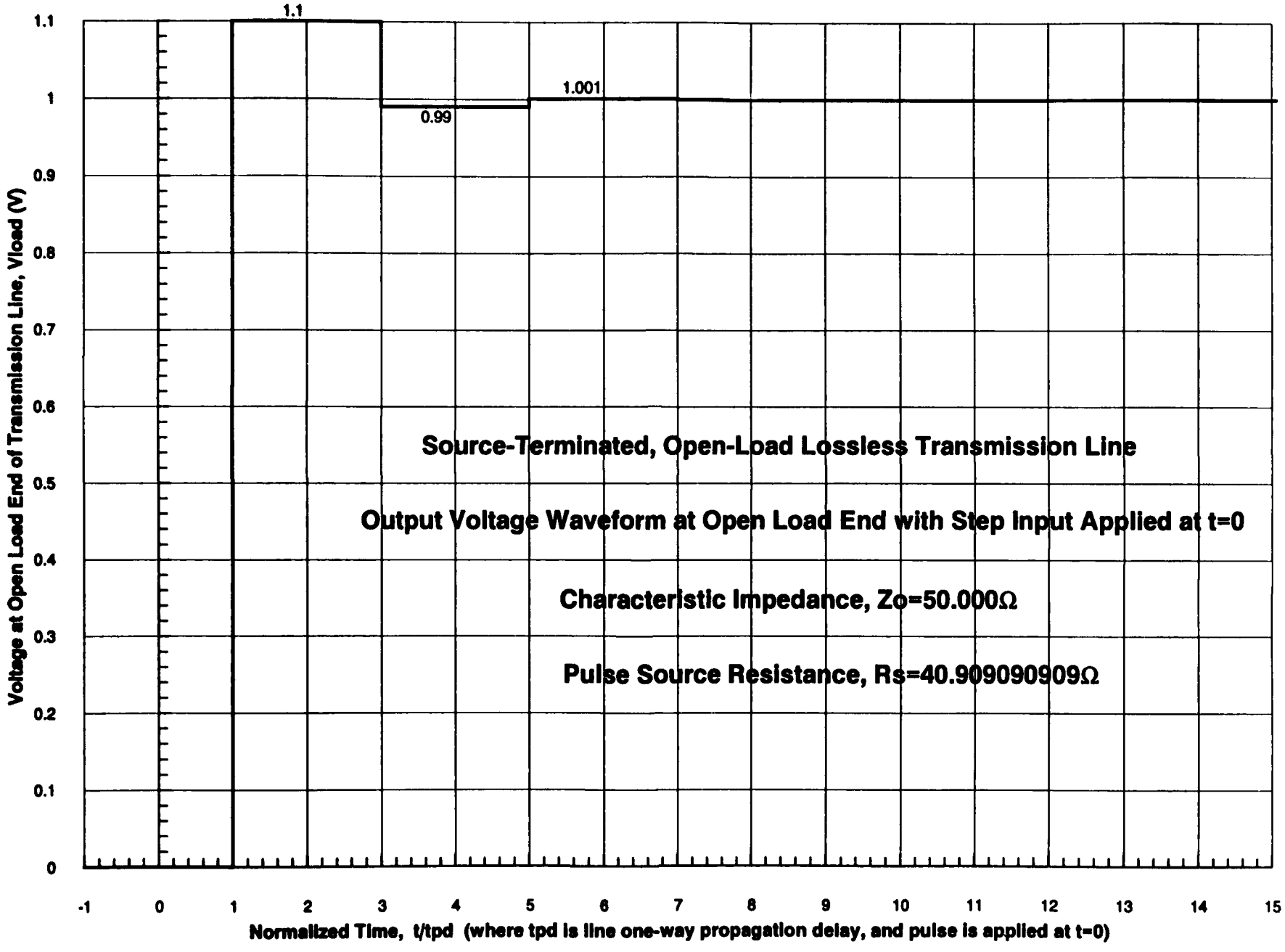

1.1
1.001
0.99
Source-Terminated, Open-Load Lossless Transmission Line
Output Voltage Waveform at Open Load End with Step Input Applied at t=0
Characteristic Impedance, Zo=50.000Ω
Pulse Source Resistance, Rs=40.909090909Ω
Voltage at Open Load End of Transmission Line, Vload (V)
Normalized Time, t/tpd (where tpd is line one-way propagation delay, and pulse is applied at t=0)
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Figure 43

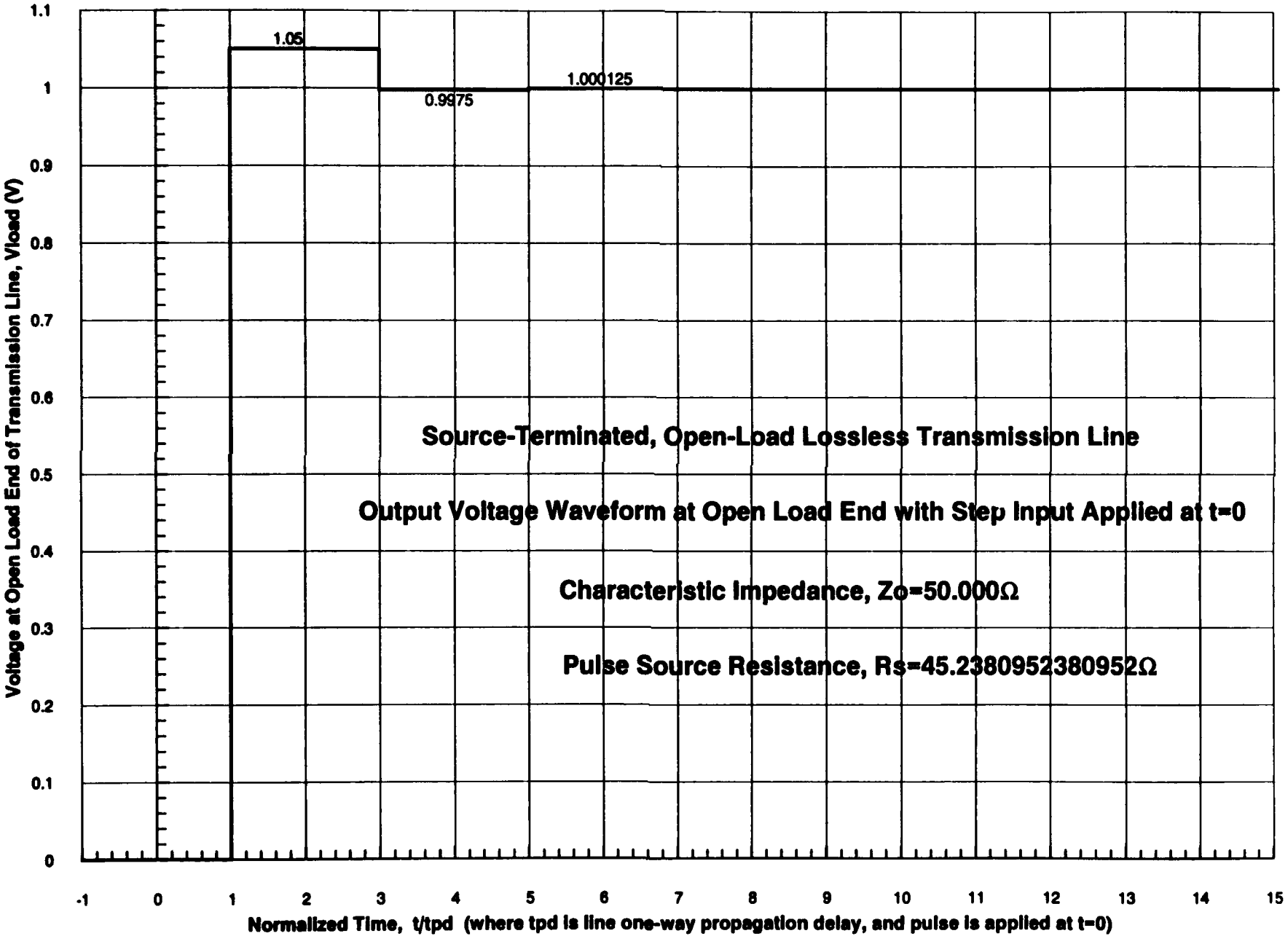

1.05
1.000125
0.9975
Source-Terminated, Open-Load Lossless Transmission Line
Output Voltage Waveform at Open Load End with Step Input Applied at t=0
Characteristic Impedance, Zo=50.000Ω
Pulse Source Resistance, Rs=45.2380952380952Ω
Voltage at Open Load End of Transmission Line, Vload (V)
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
Normalized Time, t/tpd (where tpd is line one-way propagation delay, and pulse is applied at t=0)

Figure 44

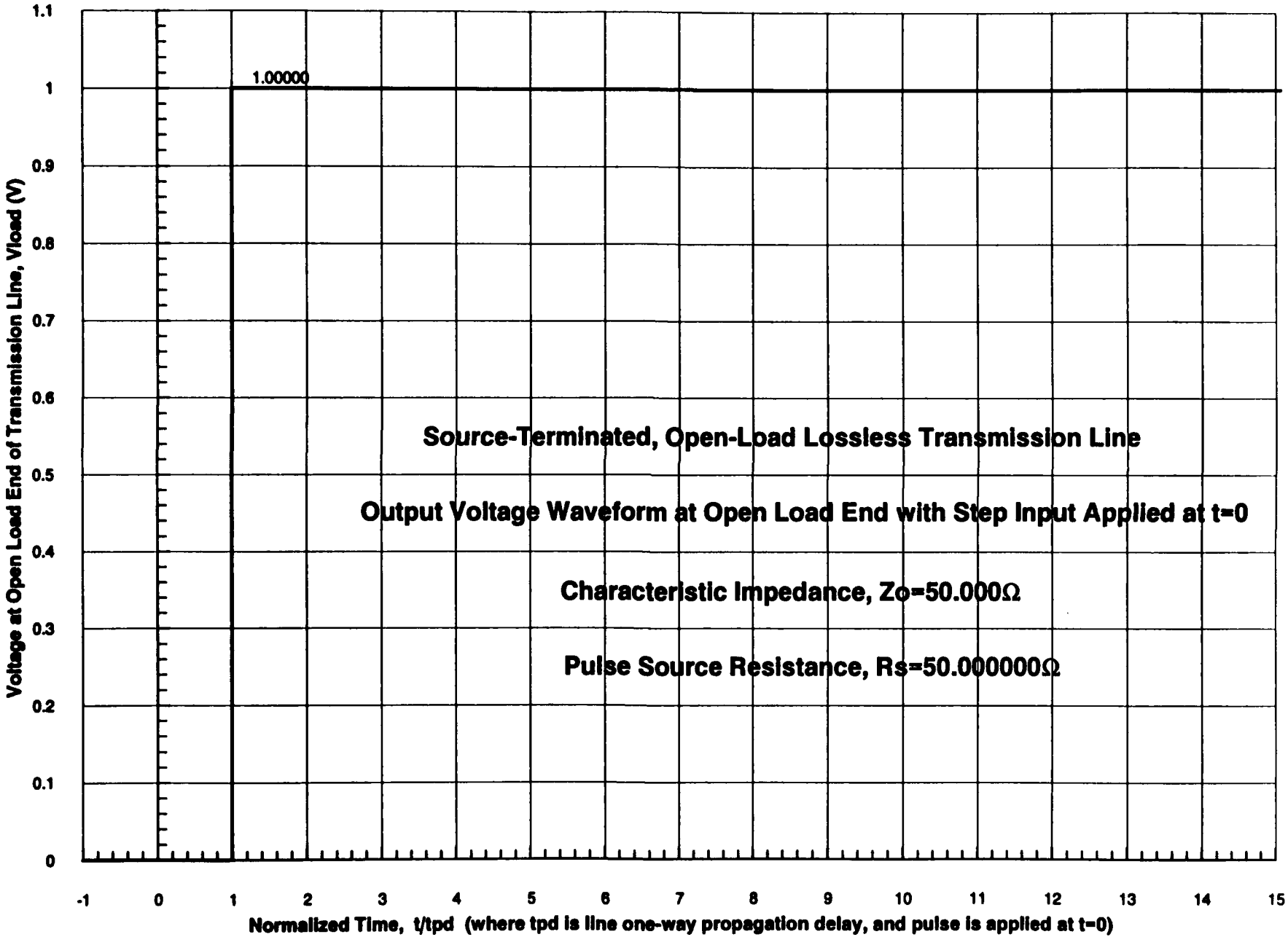

1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
1.00000
Source-Terminated, Open-Load Lossless Transmission Line
Output Voltage Waveform at Open Load End with Step Input Applied at t=0
Characteristic Impedance, Zo=50.000Ω
Pulse Source Resistance, Rs=50.000000Ω
Voltage at Open Load End of Transmission Line, Vload (V)
-1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
Normalized Time, t/tpd (where tpd is line one-way propagation delay, and pulse is applied at t=0)

Figure 45

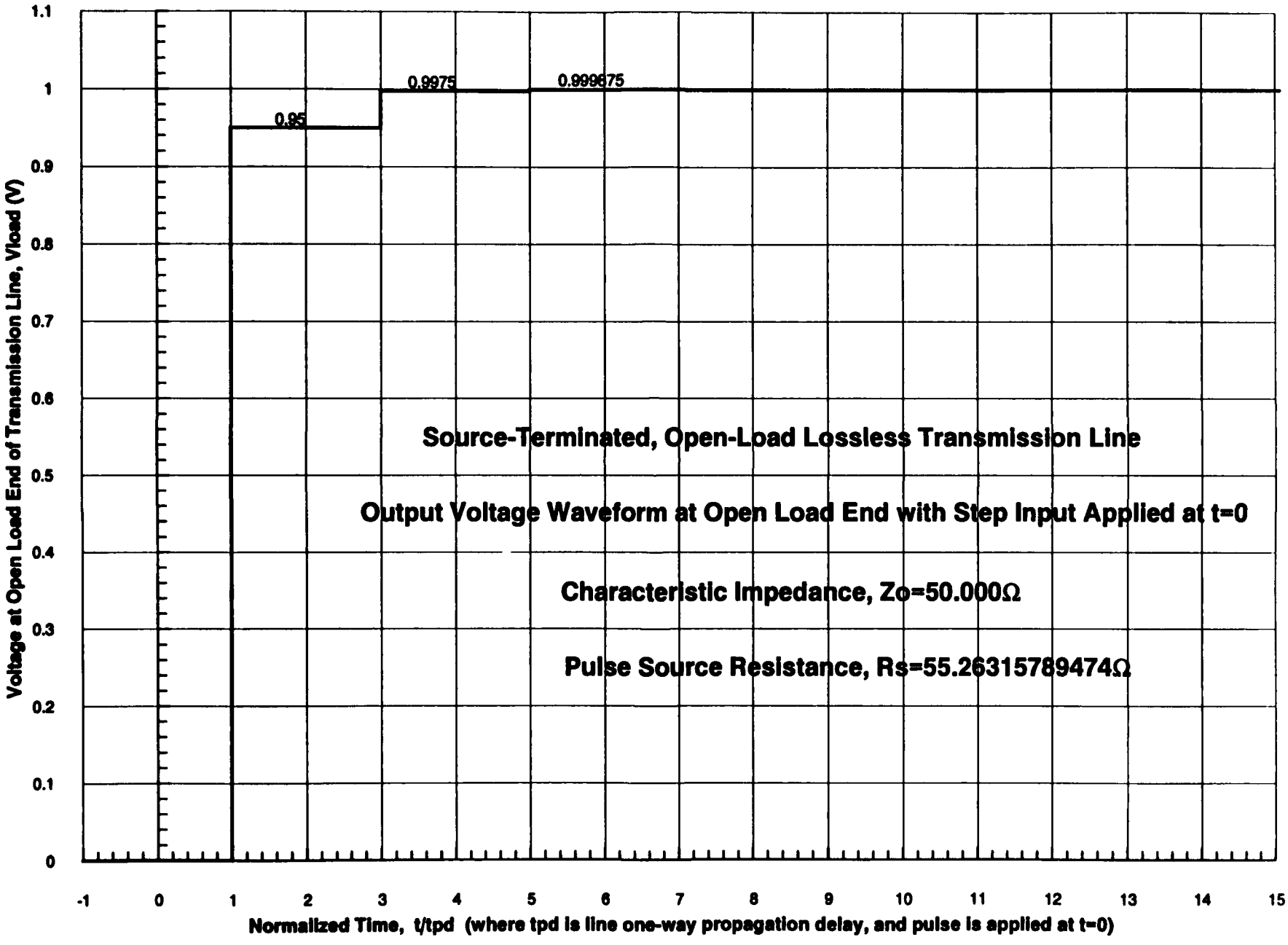

Source-Terminated, Open-Load Lossless Transmission Line
Output Voltage Waveform at Open Load End with Step Input Applied at t=0
Characteristic Impedance, Zo=50.000Ω
Pulse Source Resistance, Rs=55.26315789474Ω
0.95
0.9975
0.999875
Voltage at Open Load End of Transmission Line, Vload (V)
Normalized Time, t/tpd (where tpd is line one-way propagation delay, and pulse is applied at t=0)
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Figure 46

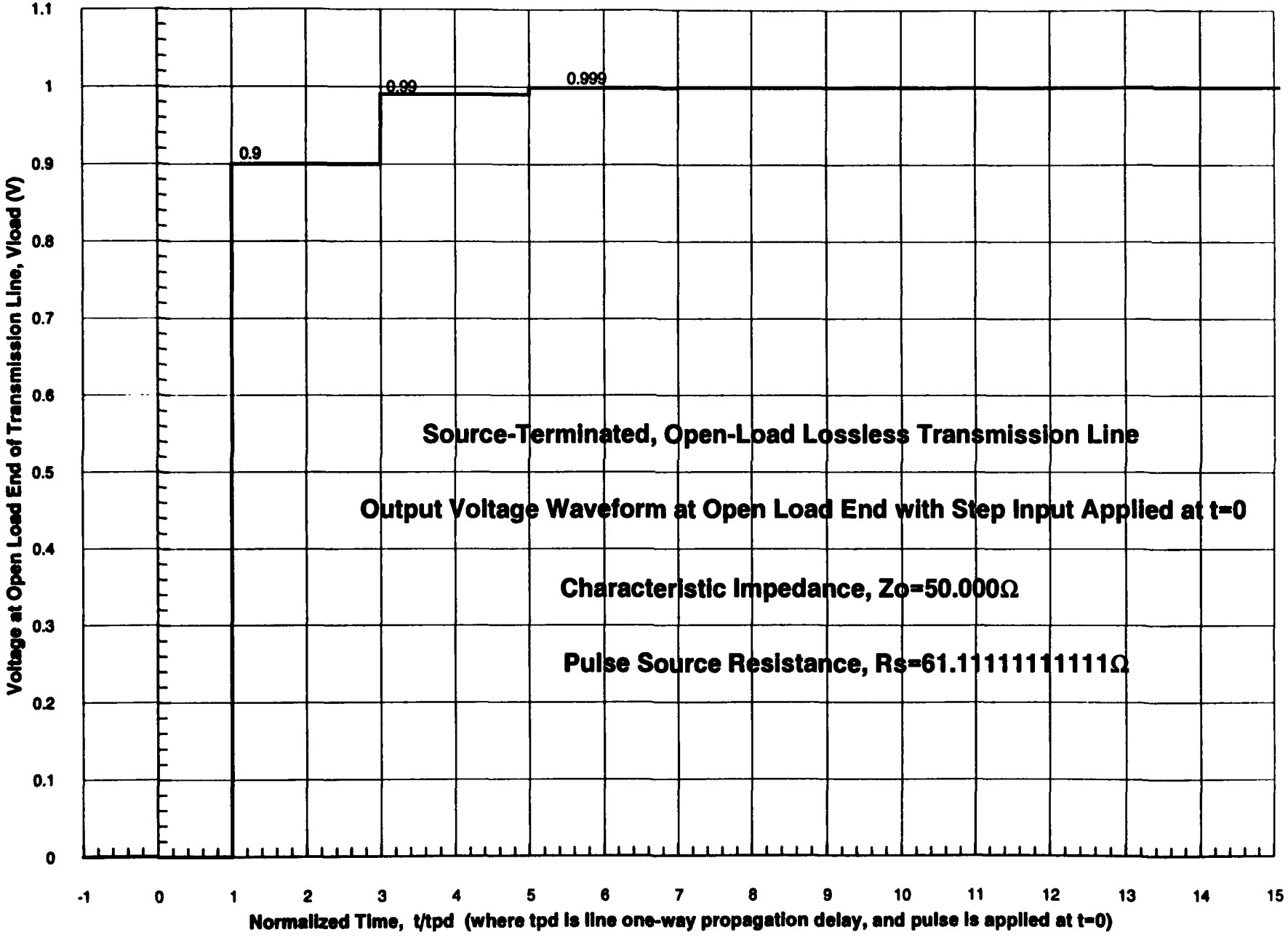

Source-Terminated, Open-Load Lossless Transmission Line
Output Voltage Waveform at Open Load End with Step Input Applied at t=0
Characteristic Impedance, Zo=50.000Ω
Pulse Source Resistance, Rs=61.11111111111Ω
0.9
0.99
0.999
Voltage at Open Load End of Transmission Line, Vload (V)
Normalized Time, t/tpd (where tpd is line one-way propagation delay, and pulse is applied at t=0)
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Figure 47

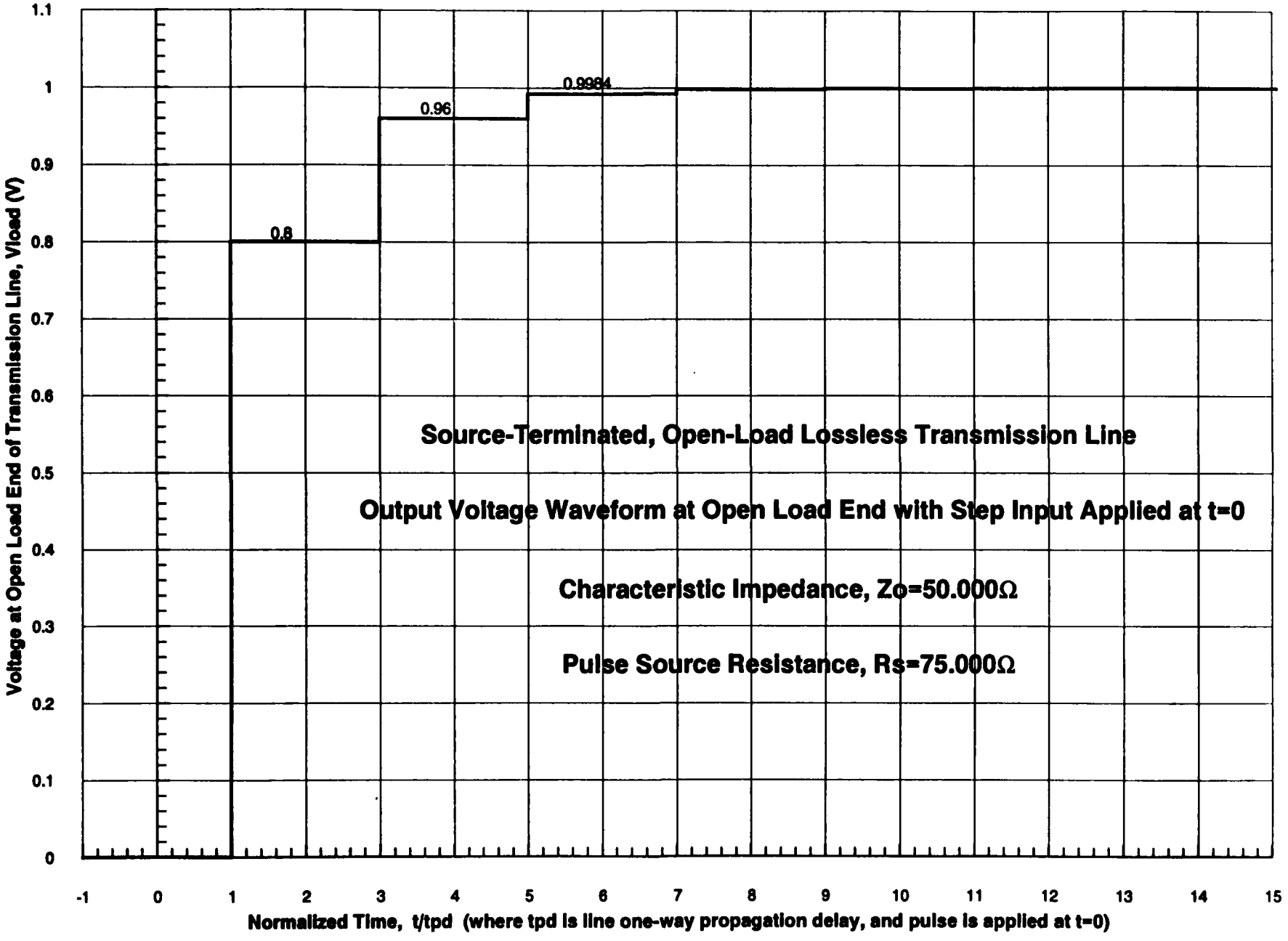

Source-Terminated, Open-Load Lossless Transmission Line
Output Voltage Waveform at Open Load End with Step Input Applied at t=0
Characteristic Impedance, Zo=50.000Ω
Pulse Source Resistance, Rs=75.000Ω
0.8
0.96
0.9984
Voltage at Open Load End of Transmission Line, Vload (V)
Normalized Time, t/tpd (where tpd is line one-way propagation delay, and pulse is applied at t=0)
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Figure 48

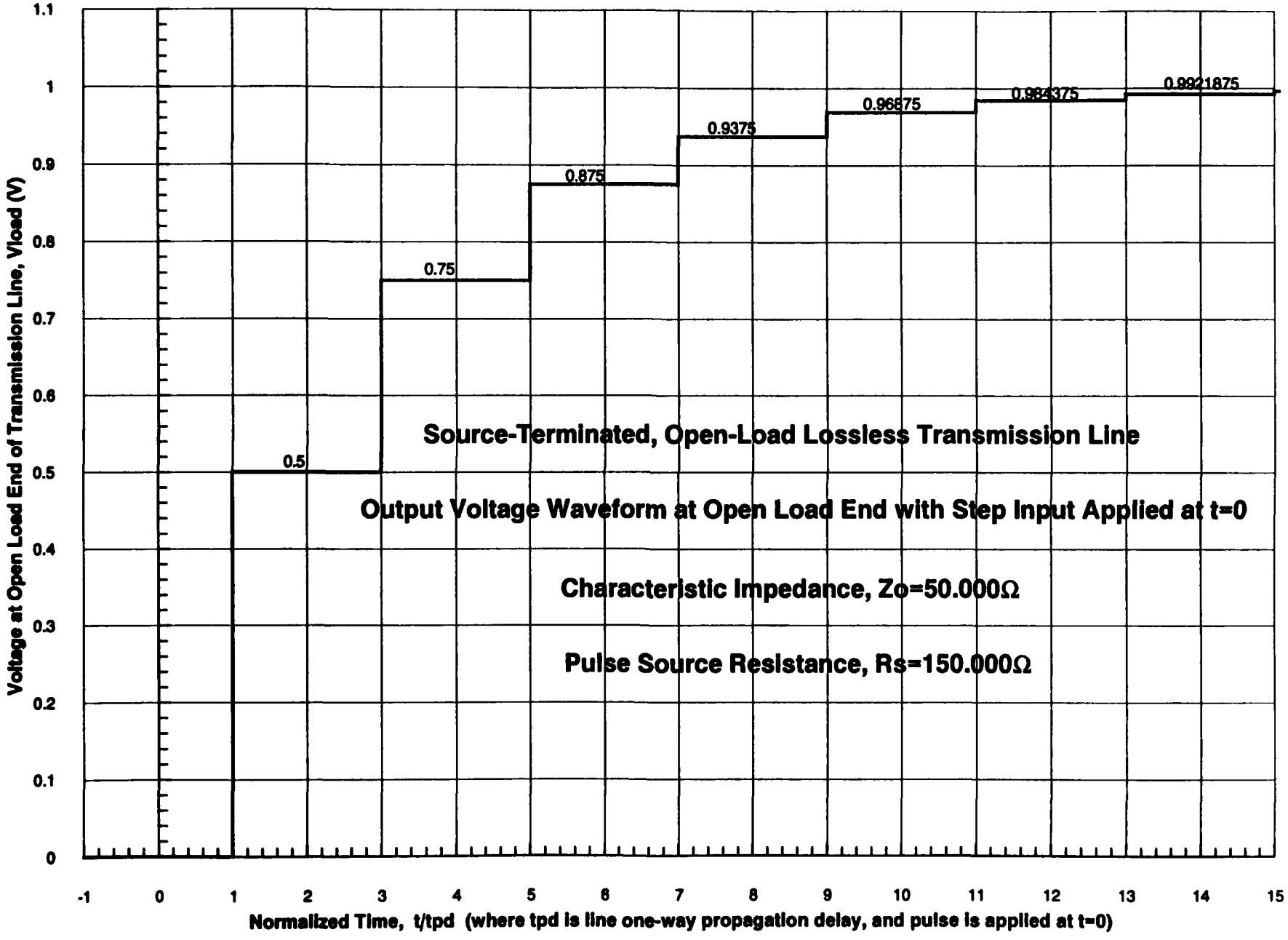

Source-Terminated, Open-Load Lossless Transmission Line
Output Voltage Waveform at Open Load End with Step Input Applied at t=0
Characteristic Impedance, Zo=50.000Ω
Pulse Source Resistance, Rs=150.000Ω
0.5
0.75
0.875
0.9375
0.96875
0.984375
0.9921875
Voltage at Open Load End of Transmission Line, Vload (V)
Normalized Time, t/tpd (where tpd is line one-way propagation delay, and pulse is applied at t=0)
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Figure 49

2.1.3. Small Lossy Coax Transient Response Simulation Examples

As discussed in the previous quarterly report, the MCM-size copper interconnect (eg. 0.25 mil to 1 mil conductors) propagation characteristics were evaluated through the example of small copper coaxial lines with a lossless dielectric of $\varepsilon_r = 3.90$ between the conductor and shield. As see in Figure 36, this makes the velocity of propagation of a lossless line equal to $v_p = 1.518 \times 10^8$ meters/s or the unit delay $1/v_p = 167.3$ ps/inch. For a 12 inch long interconnect, the nominal delay will be $\tau_{pd} = 2.0078$ ns, or for a 6" line, $\tau_{pd} = 1.004$ns, etc. The nominal characteristics impedance of the coax lines is kept at $Z_o = 50\Omega$ nominal for all line sizes. This means that if the conductivity of copper were infinite, that the line characteristic impedance would be $Z_o = 50.00000\Omega$ at any frequency. It is a reasonable approximation to the high frequency Z_o of the real coax lines where the skin effect depth is small compared to the conductor sizes. At lower frequencies, the current density spreads deeper into the conductors, increasing the internal inductance component of the line inductance (Equations 5, 10 , 12, 37, 41 and 46), which makes the Z_o a complex frequency dependent quantity. The fact that the magnitude of Z_o is higher at low frequencies than the nominal 50Ω value is why the $R_{in} = 50\Omega$ curve in Figure 50 actually shows an overshoot of 2.18% near $t = 3\tau_{pd}$, instead of the -0.63% undershoot that would be expected at $t = 3\tau_{pd}$ from Equation 8.

Figures 50 through 56 show a composite of a large number of CPU hours of lossy line simulations using the code described in the last quarterly report. These simulations are for room temperature copper coax, with center conductor diameters of 1 mil, 0.5 mils and 0.25 mils, lengths of 12" (or 6" in Figures 55 and 56), and for a range of source resistance (R_{in}) values in the range of interest. Figures 50 and 51 (expanded time scale) represent a typical case for a 6" MCM, a 12" long line with a 1 mil center conductor diameter and having $R_{dc} = 12.19614\Omega$ dc resistance (which would be considered satisfactory for modest logic risetimes in the HTSC/normal metal interconnect MCM tradeoffs of References 5 and 6). While the initial undershoot at $\tau_{pd} < t < 3\tau_{pd}$ extrapolated to $t = \tau_{pd}$ for $R_{in} = 50\Omega$ Figure 50, as seen in Figure

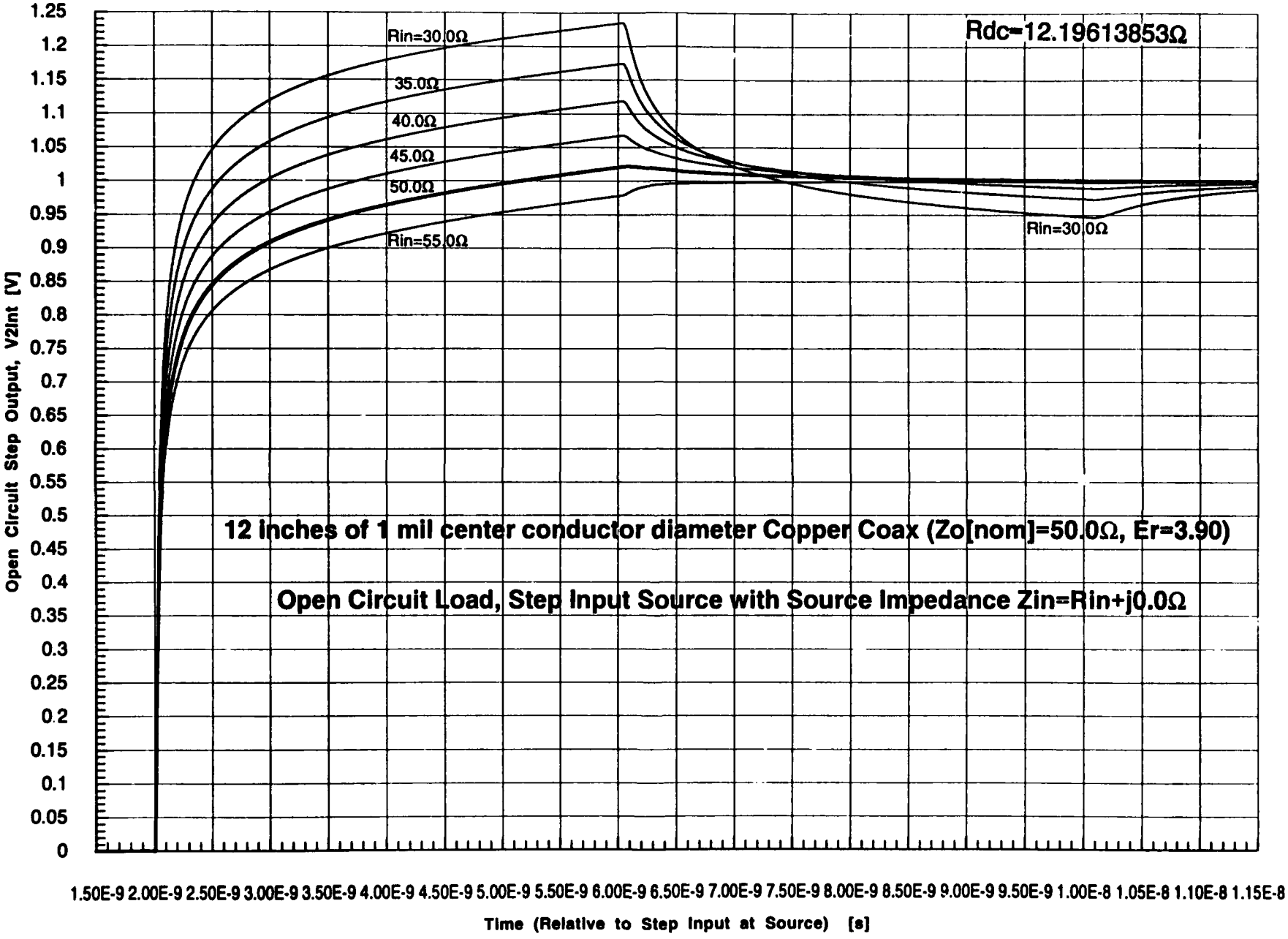

Rdc=12.19613853Ω
Rin=30.0Ω
35.0Ω
40.0Ω
45.0Ω
50.0Ω
Rin=55.0Ω
Rin=30.0Ω
12 inches of 1 mil center conductor diameter Copper Coax (Zo[nom]=50.0Ω, Er=3.90)
Open Circuit Load, Step Input Source with Source Impedance Zin=Rin+j0.0Ω
Open Circuit Step Output, V2int [V]
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
1.50E-9 2.00E-9 2.50E-9 3.00E-9 3.50E-9 4.00E-9 4.50E-9 5.00E-9 5.50E-9 6.00E-9 6.50E-9 7.00E-9 7.50E-9 8.00E-9 8.50E-9 9.00E-9 9.50E-9 1.00E-8 1.05E-8 1.10E-8 1.15E-8
Time (Relative to Step Input at Source) [s]

Figure 50

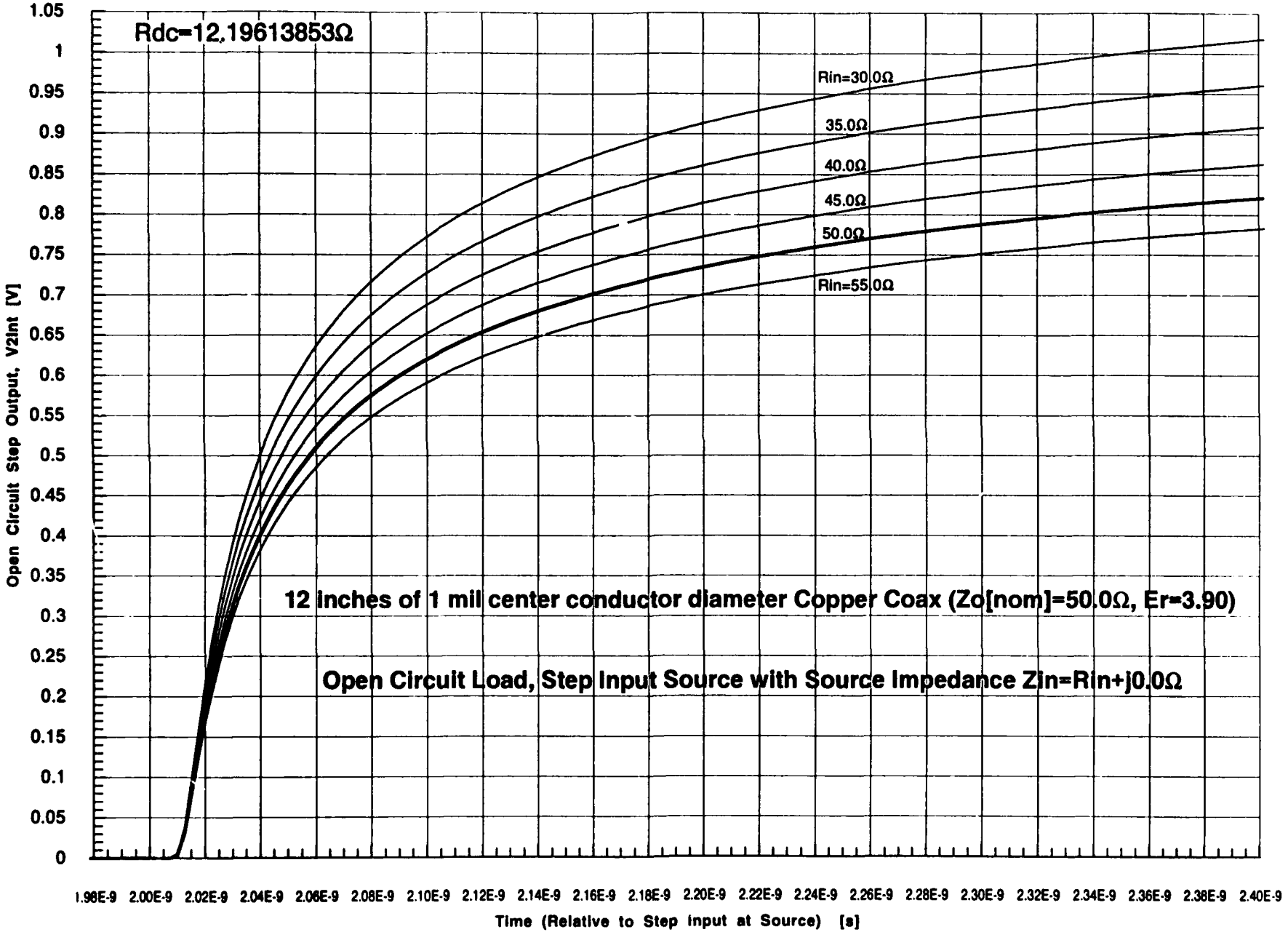

Rdc=12.19613853Ω
Rin=30.0Ω
35.0Ω
40.0Ω
45.0Ω
50.0Ω
Rin=55.0Ω
12 inches of 1 mil center conductor diameter Copper Coax (Zo[nom]=50.0Ω, Er=3.90)
Open Circuit Load, Step Input Source with Source Impedance Zin=Rin+j0.0Ω
Open Circuit Step Output, V2Int [V]
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
1.98E-9 2.00E-9 2.02E-9 2.04E-9 2.06E-9 2.08E-9 2.10E-9 2.12E-9 2.14E-9 2.16E-9 2.18E-9 2.20E-9 2.22E-9 2.24E-9 2.26E-9 2.28E-9 2.30E-9 2.32E-9 2.34E-9 2.36E-9 2.38E-9 2.40E-9
Time (Relative to Step Input at Source) [s]

Figure 51

51, the skin effect loss slows the leading edge of the step response substantially. While the center crossing is delayed less than 0.05ns, the $V_{out} = 90\% V_{in}$ crossing is not reached until about 1.9ns after the nominal pulse arrival time.

Figures 52 and 53, for 0.5 mil center conductor copper coax, 12" long shows how bad the situation gets with higher resistance lines ($R_{dc} = 48.7846\Omega$ there). With $R_{in} = 50\Omega$, the 50% crossing is reached in 0.22ns, but the 90% level crossing (the nominal risetime measurement point) is not reached until 3.25ns after the nominal pulse arrival time. As seen in Figure 52, adopting the "self-terminating" approach of reducing R_{in} to 20Ω, for example, reduces the delay to the 90% point to 0.5ns, but causes a 20% overshoot at $\tau \approx 3\tau_{pd}$ (and which for shorter lines, as seen in Figure 37 could reach a 42.8% overshoot if the R_{in} values were made equal for all lines). These issues will be discussed in greater detail in the final report.

If the conductor size is scaled down further to a 0.25 mil (6.35μm) center conductor diameter, the pulse characteristics for the 12" line, shown in Figure 54 are very bad, and cannot be made reasonable even if the source resistance, $R_{in} = 50\Omega$ is nearly 10ns, 5 times the nominal propagation delay of the line.

Shorter lines, such as the 6" case shown in Figures 55 and 56 for a 0.5 mil center conductor diameter, can tolerate somewhat smaller diameters. Here the nominal $R_{in} = 50\Omega$ delay is about 0.85ns, nearly as long as the line delay. This can be reduced by reducing R_{in}, but only at the expense of overshoot. In this case, the R_{dc} value is nearly 25Ω, which would appear to be near the allowable limit if reasonably tight overshoot specifications (eg. 5 to 10% or so) are to be maintained.

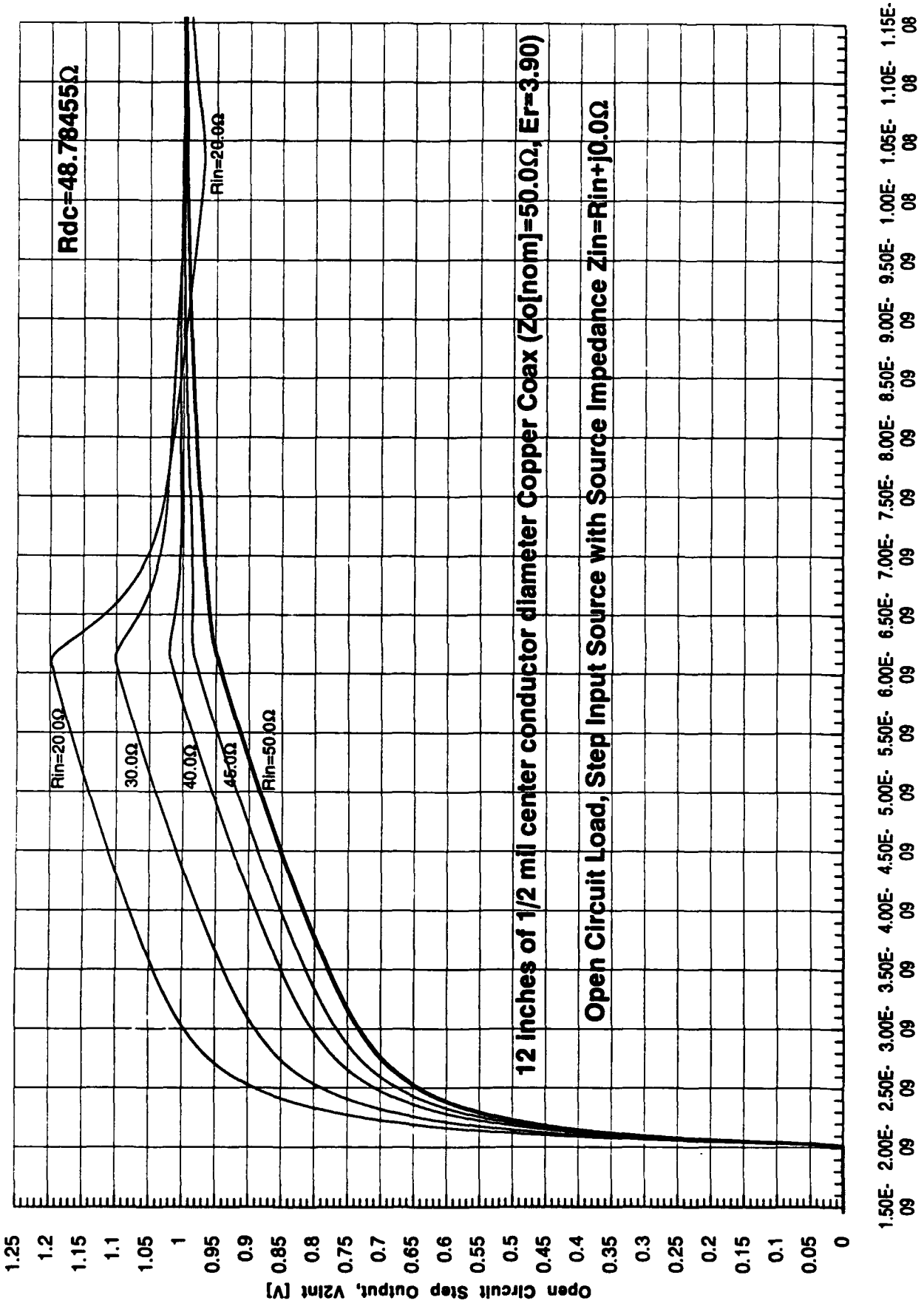

Rdc=48.78455Ω
12 inches of 1/2 mil center conductor diameter Copper Coax (Zo[nom]=50.0Ω, Er=3.90)
Open Circuit Load, Step Input Source with Source Impedance Zin=Rin+j0.0Ω
Rin=20.0Ω
30.0Ω
40.0Ω
45.0Ω
Rin=50.0Ω
Rin=20.0Ω
Open Circuit Step Output, V2int [V]
Time (Relative to Step Input at Source) [s]

Figure 52

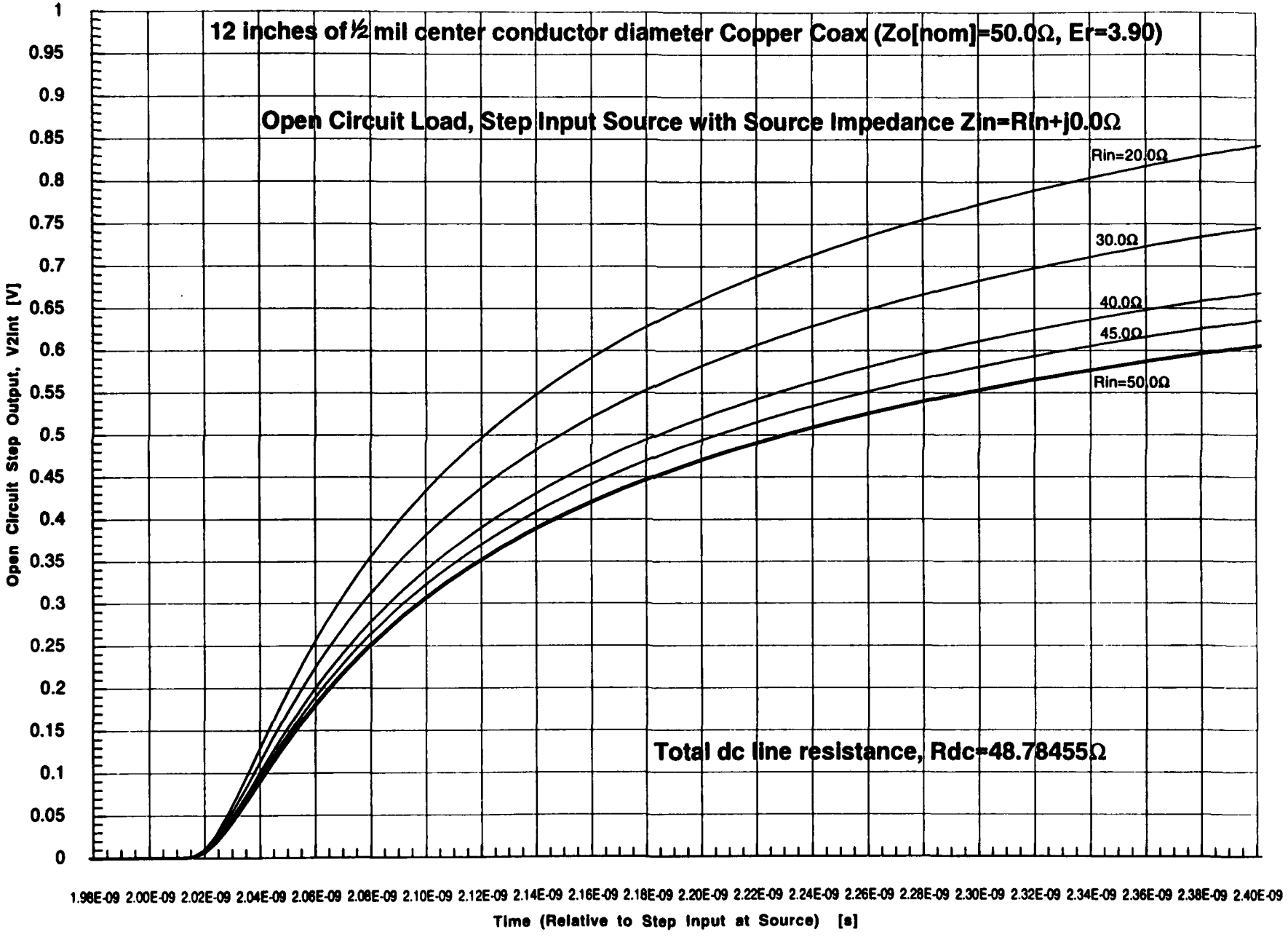

12 inches of ½ mil center conductor diameter Copper Coax (Zo[nom]=50.0Ω, Er=3.90)
Open Circuit Load, Step Input Source with Source Impedance Zin=R[n+j0.0Ω
Rin=20.0Ω
30.0Ω
40.0Ω
45.0Ω
Rin=50.0Ω
Total dc line resistance, Rdc=48.78455Ω
Open Circuit Step Output, V2int [V]
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
1.98E-09 2.00E-09 2.02E-09 2.04E-09 2.06E-09 2.08E-09 2.10E-09 2.12E-09 2.14E-09 2.16E-09 2.18E-09 2.20E-09 2.22E-09 2.24E-09 2.26E-09 2.28E-09 2.30E-09 2.32E-09 2.34E-09 2.36E-09 2.38E-09 2.40E-09
Time (Relative to Step Input at Source) [s]

Figure 53

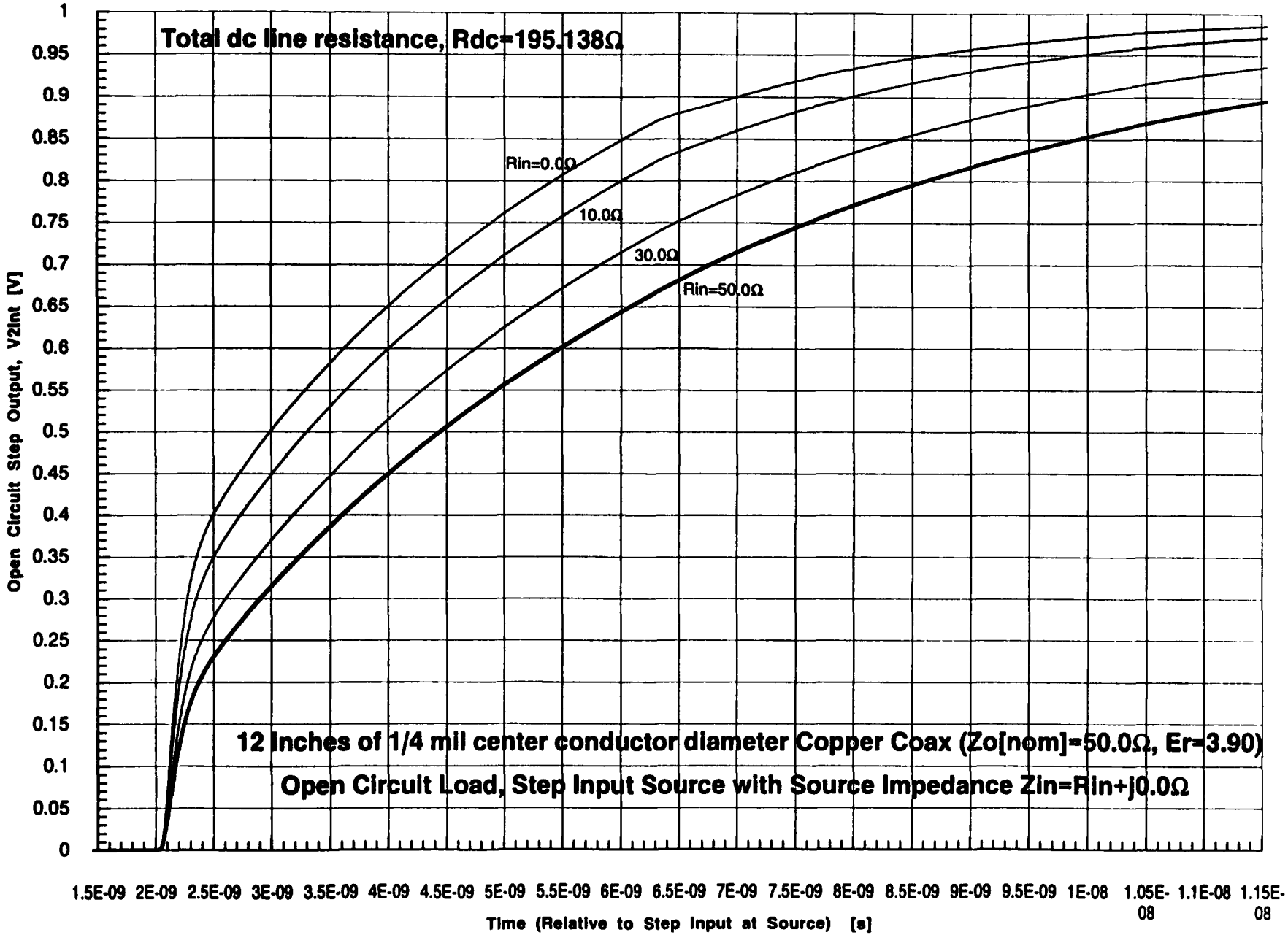

Total dc line resistance, Rdc=195.138Ω
Rin=0.0Ω
10.0Ω
30.0Ω
Rin=50.0Ω
12 inches of 1/4 mil center conductor diameter Copper Coax (Zo[nom]=50.0Ω, Er=3.90)
Open Circuit Load, Step Input Source with Source Impedance Zin=Rin+j0.0Ω
Open Circuit Step Output, V2int [V]
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
1.5E-09 2E-09 2.5E-09 3E-09 3.5E-09 4E-09 4.5E-09 5E-09 5.5E-09 6E-09 6.5E-09 7E-09 7.5E-09 8E-09 8.5E-09 9E-09 9.5E-09 1E-08 1.05E-08 1.1E-08 1.15E-08
Time (Relative to Step Input at Source) [s]

Figure 54

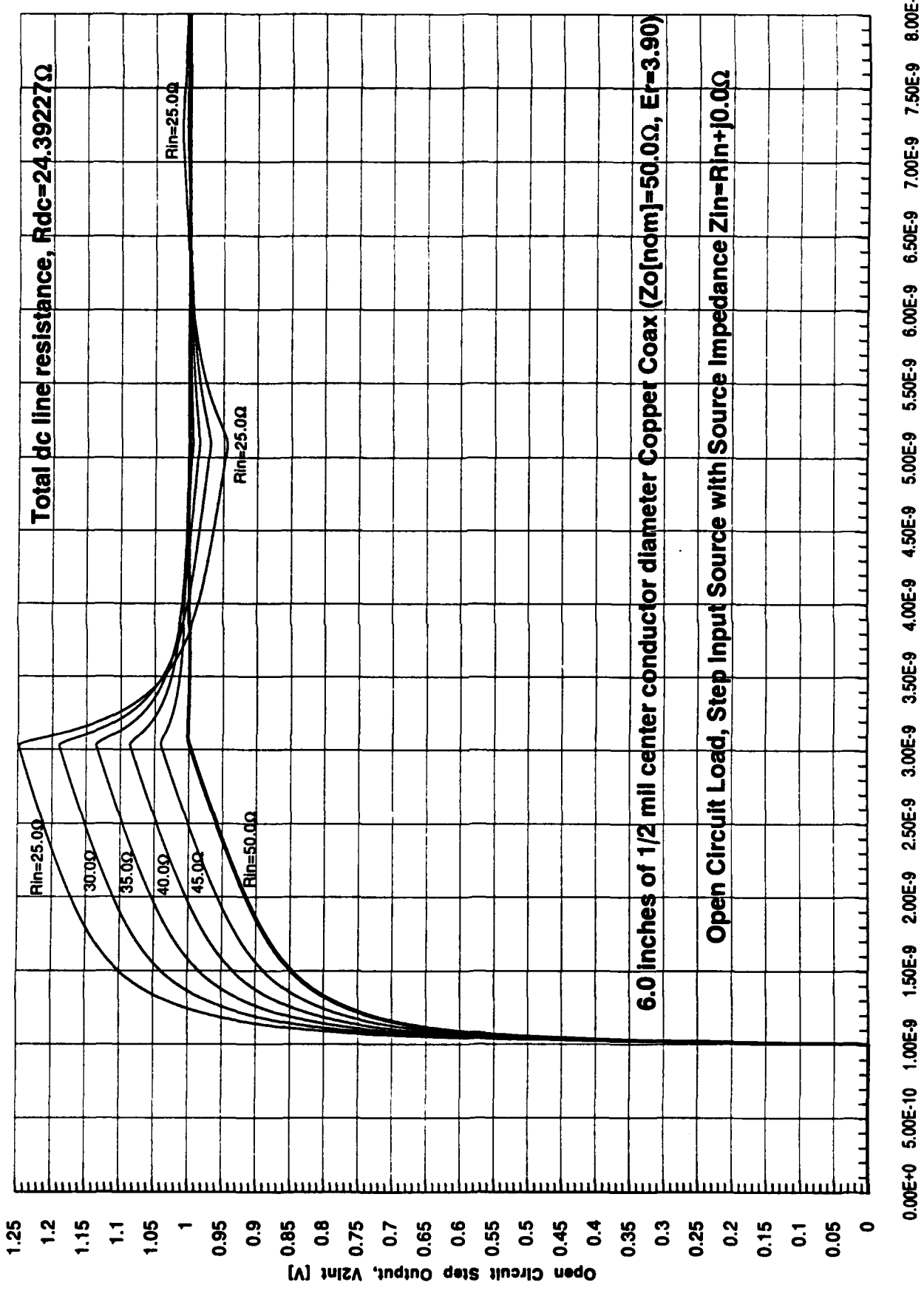

Total dc line resistance, Rdc=24.39227Ω
6.0 inches of 1/2 mil center conductor diameter Copper Coax (Zo[nom]=50.0Ω, Er=3.90)
Open Circuit Load, Step Input Source with Source Impedance Zin=Rin+j0.0Ω
Rin=25.0Ω
30.0Ω
35.0Ω
40.0Ω
45.0Ω
Rin=50.0Ω
Rin=25.0Ω
Rin=25.0Ω
Open Circuit Step Output, V2int [V]
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0.00E+0
5.00E-10
1.00E-9
1.50E-9
2.00E-9
2.50E-9
3.00E-9
3.50E-9
4.00E-9
4.50E-9
5.00E-9
5.50E-9
6.00E-9
6.50E-9
7.00E-9
7.50E-9
8.00E-9
Time (Relative to Step Input at Source) [s]

Figure 55

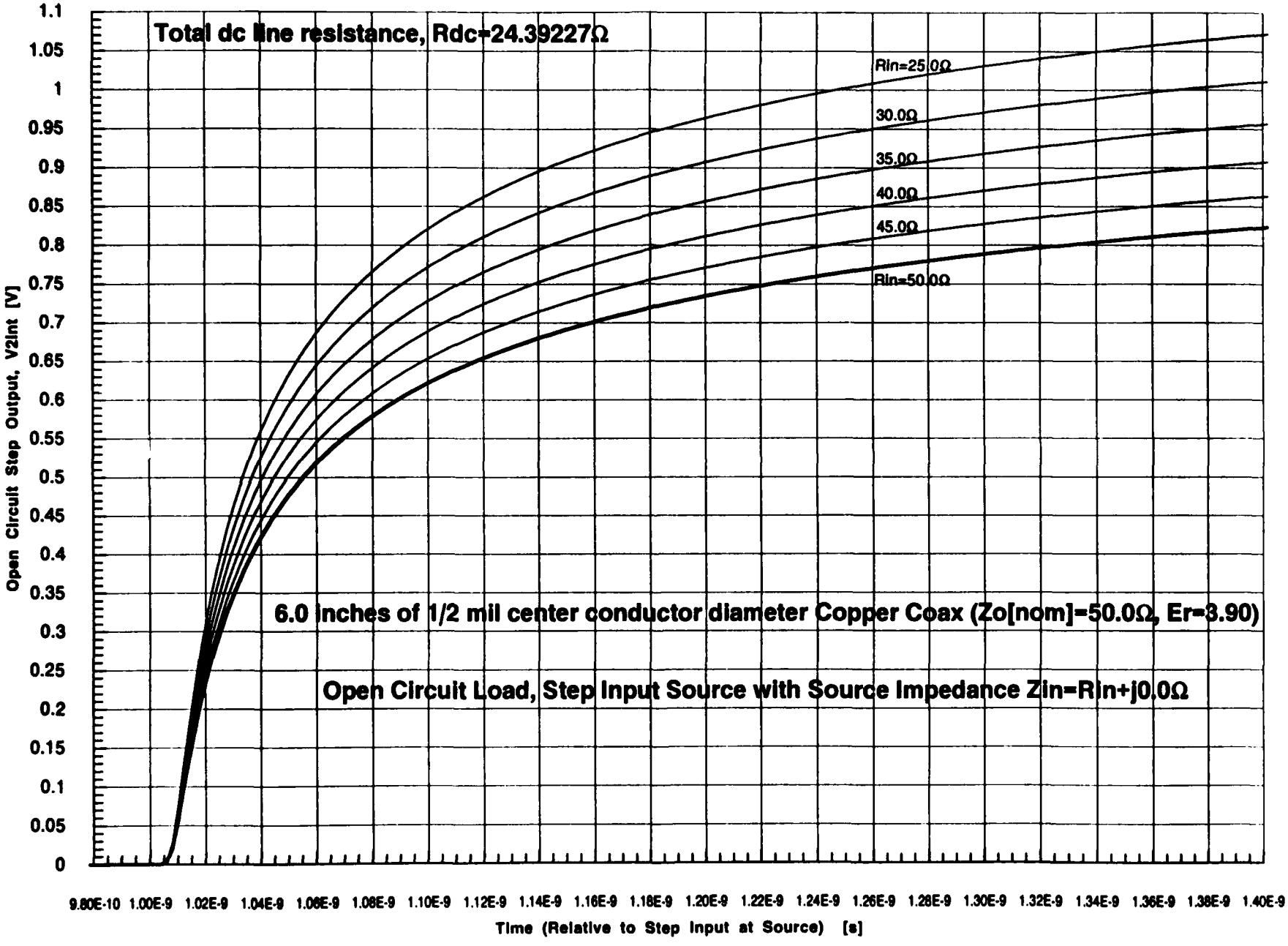

Total dc line resistance, Rdc=24.39227Ω
Rin=25.0Ω
30.0Ω
35.0Ω
40.0Ω
45.0Ω
Rin=50.0Ω
6.0 inches of 1/2 mil center conductor diameter Copper Coax (Zo[nom]=50.0Ω, Er=3.90)
Open Circuit Load, Step Input Source with Source Impedance Zin=Rin+j0.0Ω
Open Circuit Step Output, V2int [V]
1.1
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
9.80E-10 1.00E-9 1.02E-9 1.04E-9 1.06E-9 1.08E-9 1.10E-9 1.12E-9 1.14E-9 1.16E-9 1.18E-9 1.20E-9 1.22E-9 1.24E-9 1.26E-9 1.28E-9 1.30E-9 1.32E-9 1.34E-9 1.36E-9 1.38E-9 1.40E-9
Time (Relative to Step Input at Source) [s]

Figure 56

2.2. Commercial Applications

This past quarter has seen a slight shift in emphasis. The question we were asking is this: What will it take the system designers to use conventional room temperature MCM and then from there why will he use cryoelectronic MCM?

An interesting answer came out of this type of questioning. First, we find that IC's are optimized for single packages not for MCM applications. If we can optimize IC for MCM we will gain on at least two grounds relating to both yield and performance enhancement. First we can partition chips to smaller sizes, mount them on MCM and not lose much if any in performance, but gain significantly in price. Large chips in production at extremely low yields can be produced at significantly lower prices if they are partitioned at smaller sizes, since smaller chips will be produced at much higher yields. The second point is that many logic chips are now I/O limited, by producing chips with area distributed I/O significant simplification in design and enhancement in performance will result. Therefore, we think IC's could lead to cheaper and higher performance systems.

It then becomes obvious that where we optimize IC's for cryoelectronic applications, we need to optimize them also for MCM's. This approach could really result in a major compelling reason to use cryoelectronics.

SECTION 3

APPENDICES
PREVIOUS QUARTERLY REPORTS

3.1 Q4 1991 Quarterly Report

Section 1.0

1.1 Introduction

The focus of the effort described in this report is updating and extending the analysis of the number of signal layers required for a square 2-D MCM fabricated from 10 K-gate, 0.6 cm square chips, flip-chip mounted with maximal density. The analysis follows that of Ref. 7 (which treated the 30 K-gate, 1 cm chip case) in treating both 300°K and 77°K cases, and both standard high speed R_{max} = 10Ω and compromised, self-terminated R_{max} = 25Ω cases. It should be noted that the text of Section 1.3 is largely reproduced from Ref 1, however, the analytical results obtained in this report are new and relate to the previously mentioned extensions. The analysis is extended to include plots of the required thickness of the interconnect mat for various signal frequencies, as well as the number of signal layers required to complete the inter-chip wiring. For completeness, a short background (Ref. 7) is included as Section 1.2.

1.2 Background

Since nearly the advent of integrated circuit technology, the vision has been to bypass the great expense and performance compromises of multi-level packaging by implementing entire systems (or major portions thereof) on a single IC wafer. Unfortunately, a number of technical realities mitigate against such a wafer-scale integration approach, at least for general purpose digital systems. The principal problem is yield, and the very high overhead costs of coping with this through redundancy, but perhaps equally important are issues of process and design optimization. Manufacturers of a specific ultra high density DRAM chip could not be expected to achieve the same cost, density and performance levels if the function had to be created as a part of a larger general-purpose logic design. These, and other, practical considerations have modified the focus away from the single

semiconductor substrate wafer scale integration vision to the "hybrid wafer scale" concept in which virtually the same density goals are achieved in a multi-chip module (MCM) virtually "tiled" with VLSI die, as illustrated in Fig. 1. Multi-chip modules (MCMs) are an advanced form of hybrid integrated circuit developed to meet the special needs of complex high density digital systems. Specifically, MCMs have large numbers of integrated circuit (IC) die, each having a large number of I/Os (signal input/output connections), which makes the density of inter-chip interconnections very high.

It is now generally accepted that performance, and potentially cost, reasons, the coming wave in electronics packaging is the multi-chip module (MCM). In MCM packaging technology [see Refs. 1-4], bare integrated circuit die are attached, both physically (chip bonded) and electrically (pad bonded), to a substrate which carries some type of multi-layer interconnect system to provide for the power connections to the die and the large number of signal interconnections required between the various chips on the MCM, and to the "outside world". The MCM, which may contain anywhere from a few IC chips to over a hundred in current MCM practice (and which may be expected to increase to many hundreds, as shown in Fig. 1, and possibly the low thousands in the future), represents the first-level package for the IC die. By eliminating the requirement for a large number of individual IC packages, the MCM allows for major reduction in size and weight in electronic systems (and potentially reduction of cost).

One of the key derivative benefits of MCM technology, which is a consequence of the reduction in size, is a major reduction of signal propagation delay or signal latency. In transmission lines, the propagation velocity of signal pulses is limited by the speed of light divided by the square root of the average dielectric constant of the dielectric(s) between the signal line and ground plane(s) [Eq. 1]. The total pulse delay is, of course, not less than the line length divided by this velocity. The very small distances between IC chips in MCM's (as compared to circuit board packaging) greatly reduce this propagation delay. Since in most digital systems the maximum clock frequency is limited to the reciprocal of the sum of the logic circuit delay plus this signal interconnect propagation delay, reduced propagation delays

Maximal-Density HTSC MCM "System on a Substrate"

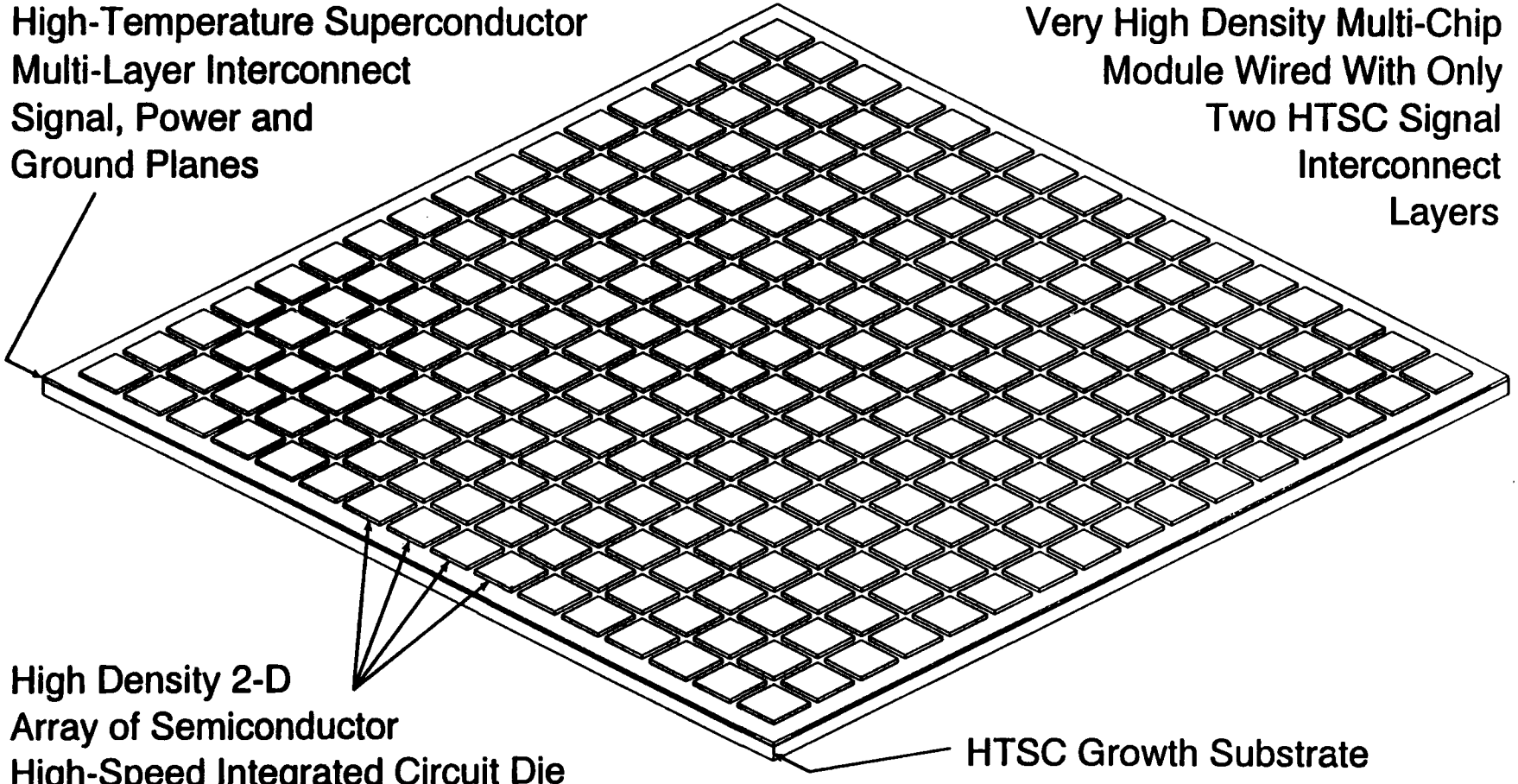


Figure 1

translate into higher system speeds, particularly if the logic speeds can be increased as well. Of course, the major direction of thrust in the semiconductor/IC industry has been to increase chip speeds. This is rather dramatically illustrated by the fact that the fastest supercomputer available in 1980, the CRAY1, had an 80MHz clock rate (and $10 million price). In comparison, the Macintosh FX on which most of the work on this project was done was purchased in 1990 for under one thousandth of price of a CRAY1, but in fact runs at a 40 MHz clock rate, half that of a CRAY1. Hence we see that today, even in less expensive CMOS applications, the reduced interconnect delays afforded by MCMs are precisely what digital system designers need to translate the escalating IC speeds into greatly improved system performance.

The simplest concept for a large MCM would be to use normal semiconductor processing (two to four layers of metal interconnects with typically $\approx 1\mu$m signal linewidths) on a large (4" to 6" or larger) wafer to serve as the inter-chip connection medium in the MCM. Unfortunately, even a 4" square MCM would have up to 8" long signal lines, which, assuming a 1μm x $0.5\,\mu$m cross section and a $\rho = 1.7 \times 10^{-6}$ ohm cm metal resistivity (for copper; aluminum would be worse), the line resistance would be $R_{max} = 6900$ ohms. This is two or three orders of magnitude too large to be useable for interconnects in a high speed digital system.

All signal interconnects in digital systems are, for better or for worse, transmission lines. Signal lines implemented with normal metal conductors can usually be approximated as an ideal distributed L-C line with a conductor resistance in series with each inductor (this ignores the dielectric losses). In the ideal case when the total signal line resistance is very small in comparison to the line impedance, $R_{line} << Z_o$, the waveform integrity is excellent and the velocity of propagation, v_p, is just given by

$$v_p = c / \sqrt{\varepsilon_r} \qquad \text{Eq. 1}$$

where ε_r is the average dielectric constant in the line. Since the line impedances normally employed are in the range of $Z_o = 50\Omega$ (or within a factor of 2 of this), clearly the 8" long, W = 1 μm copper line ($R_{line} = 6900\Omega$) case cited above is far from this ideal case. Note that for $R_{line} >> Z_o$, the propagation approaches a distributed R-C line characteristic which exhibits so-called "telegrapher's delay" or signal "diffusion" characteristics, with gross distortion, risetime degradation and long signal delays [see Ref. 4, Sect. 5.2, pp. 198-211]. While the exact tolerance to interconnect line resistance depends on details of the application, in general, $R_{line} < 10\Omega$ is quite satisfactory, even for ECL-type ($R_{load} = Z_o = 50\Omega$ load-terminated) interconnection approaches, with slightly higher ohmic line resistances tolerable in source-terminated (CMOS-like) approaches.

The basic problem with the use of normal metal interconnects in large, complex MCMs is that (because of the substantial metal resistivity) the conductor areas required to keep the end-to-end ohmic line resistances under 10Ω make it extremely difficult to achieve the wiring densities needed. In fact, the only way to approach the wiring densities needed with normal metal conductors is to increase the number of signal interconnect layers, often (as will be shown in Section 1.3) to impractically large numbers for maximal-density complex MCMs. Since a superconductor behaves, to a large extent, like a conductor with essentially zero resistivity, much finer conductor linewidths (limited mainly by lithography) could be used for such applications. However, the fabrication of complex MCMs, even with the most convenient and easy to use materials, is challenging from yield and manufacturability standpoints, and high temperature superconductor (HTSC) materials are certainly not convenient and easy to use from an MCM fabrication standpoint. Hence the first question to address regarding the application of HTSC interconnects to complex MCMs is "Is this trip really necessary?". This question is addressed in Section 1.3, using quantative analysis tools and techniques developed previously in this effort and described in detail in Ref. 1.

1.3 Analysis Approach/Nominal 300°K Cu to HTSC Comparison Results

The studies and analysis discussed above, and in Refs. 1 and 7, indicate that there are strong advantages for the use of high temperature superconductors for the signal interconnections in large, very high density 2-dimensional multi-chip modules of the type illustrated in Fig 1. In particular, Section 3.1 of Ref. 1 describes in detail the technique of analysis of the number of signal interconnect layers versus MCM size required to complete the inter-chip wiring for maximal density (surface "tiled" with IC chips with minimal spacing between them) square MCMs (eg., Fig. 1). The comparison, between copper (room temperature in Ref. 1 and expanded in Ref.7 and Section 1.4 here to include 77°K Cu) and HTSC interconnect materials, is based on a number of assumptions. These assumptions include: 1) chip I/O counts determined from Rent's rule as published by IBM [Ref. 2, page 14, Fig 1-7] for high performance chips (eg. 370 I/O's for a 10,000 gate chip, taken to be 0.6 cm square), 2) average wire lengths from a Donath statistical wire length model [Ref. 3, page 64 or Ref. 4, page 430] with Rent's rule exponent of p = 2/3, 3) a conductor width of W, a thickness of $t_w = W/2$ [for fabricability] and a spacing of 3W [for low crosstalk; see Ref. 3, Ch. 3, pp. 78-124], where W is the same for all conductors and selected to meet line resistance limitations, 4) a 40% utilization of theoretical channel space by actual interconnects (40% wiring efficiency [eg., Ref. 3, page 63]), 5) the longest line does not exceed two times the MCM size (ie., corner to corner line with "Manhattan" wiring with no "wrong way" routing, 6) both dc and ac (skin-effect) signal line loss mechanisms are considered [in Ref. 1, just dc and 300MHz ac cases were treated, here extended to a range of signal risetimes/ frequencies], 7) a room temperature bulk resistivity (1.70 $\mu\Omega$-cm) value is assumed for copper, with a 77°K value 4.4x smaller, selected to give a calculated (from Eq. 7) R_{surf} at f = 1GHz equal to that measured in Ref. 5, 8) point to point wiring, making the number of wires equal to half of the total number of I/O pads, and 9) a maximum allowable resistance for the worst case line of R_{max} (where $R_{max} = 10\Omega$ is taken as adequately small in comparison to the characteristic impedance for load-terminated or source-terminated interconnects, and $R_{max} = 25\Omega$ is considered for either partially self-terminated or as a modest performance compromise in normal

source-terminated interconnects). For these specific parameters, the required number of signal layers, S, is given by (from Ref. 1, Section 3.1, Fig. 1-4)

$$S = 5R_{bar}IW/X_{chip} \qquad \text{Eq. 2}$$

where R_{bar} is the average wire length (from Donath model) measured in units of the chip mounting pitch, X_{chip}, I is the number of I/O pads per chip, W is the signal conductor width, and the constant 5 comes the product of 0.5 (wires/pad) times 4 (wire pitch/W ratio) divided by 40% (wiring efficiency). When looking at the plots of S vs. MCM size which follow, it is desirable to be able to identify the copper conductor linewidth, W, for any given point. The corresponding tables of data include the W values in cm for the f = 1.0 GHz (Tr = 400ps risetime) case, but not for dc or other signal frequencies. However, R_{bar} is given in the tables and it does not depend on signal frequency, etc., so from Eq. 2 the reader can simply use

$$W = SX_{chip}/5R_{bar}I \qquad \text{Eq. 3}$$

to get the signal line width for any other case. For a maximal-density MCM fabricated with a given chip, the mounting pitch, X_{chip}, and of course the I/O pad count, I, will be constant, and R_{bar} does not vary very strongly with MCM size, so W largely tracks the number of signal layers, S.

In Ref. 1, Section 3.1, a comparison for dc and 300MHz ac (the third harmonic of a 100MHz clock, for example, corresponding to pulse risetimes of the order of 1.3ns) signals of 300°K copper and HTSC interconnects for a maximal-density MCM is was described. The analysis indicates that under the above assumptions, taking $R_{max} = 10\Omega$, a 6-inch square MCM tiled with 10K gate, 0.6 cm square chips flip-chip mounted on a 0.635 cm pitch would hold 576 chips (24 rows and columns), but would require 62 layers of room temperature copper signal lines to complete the over 100,000 interconnects between chips (actually, that analysis treated the ac "skin effect" line losses favorably in ignoring the current crowding and ground plane loss contributions; a better estimate of the number of signal layers to keep the 300 MHz line resistances as under 10Ω is shown in the analysis presented later to be S = 92

layers for a 6" maximal density MCM). With the usual triplate configuration, (one layer of X and one layer of Y direction signal ines sandwiched between pairs of ground [reference] planes) illustrated in Fig. 2 for the case of S = 6 signal interconnect layers, the total number of metal (including ground) layers would be 93! While IBM uses 63 layers for their Enterprise System 9000 modules, these have available a full set of "E-C" (engineering change) pads on the surface with which patch and repair strategies can be executed. (These, of course, greatly reduce the number of chips that can be mounted on the MCM - eg., 121 for the 5" IBM boards). Creating defect-free boards with 93 metal layers would appear, from a manufacturing standpoint, highly un-feasible, to say the least.

With high temperature superconducting interconnects, on the other hand, this same maximal density 6" MCM can be wired using only 2 levels of signal interconnects (one "X" and one "Y"). This S = 2 case is essentially identical to standard commercial MCM configurations (eg. the nCHIP process) as illustrated in Fig. 3, except that for HTSC all dimensions are reduced by about 10X to 20X. This is possible by reducing the width of the signal lines to levels (eg., W of $\approx$ 1.5 μm$-$2μm) limited by photolithography rather than line resistance (W of $\approx$ 50 μm for copper). Obviously, even with only two signal interconnect layers it will not be easy to make the 1.9 miles of signal lines on a 6" MCM completely free of defects, but with only one X and one Y layer of lines, it should be practical to develop laser or other repair strategies to handle modest numbers of defects after completion of the boards.

The attraction of the HTSC interconnect MCM, then, is that large "system on a substrate" sized maximal density MCMs could be simply manufactured with only two signal layers (using board repair strategies to deal with material and processing defects). The payoff for putting everything in the same 1st-level (MCM) package is avoiding the large inter-package delays involved in passing through the second level (eg., circuit board level) of packaging when the IC chips must be divided among many MCMs. Since usually the interconnect delays are not more than 25% to 40% of the cycle time, simply reducing interconnect delays without corresponding reductions in the logic delays in the ICs would not buy that much in the way of system

'Silicon Circuit Board' Conventional MCM With Six Signal Interconnect Layers

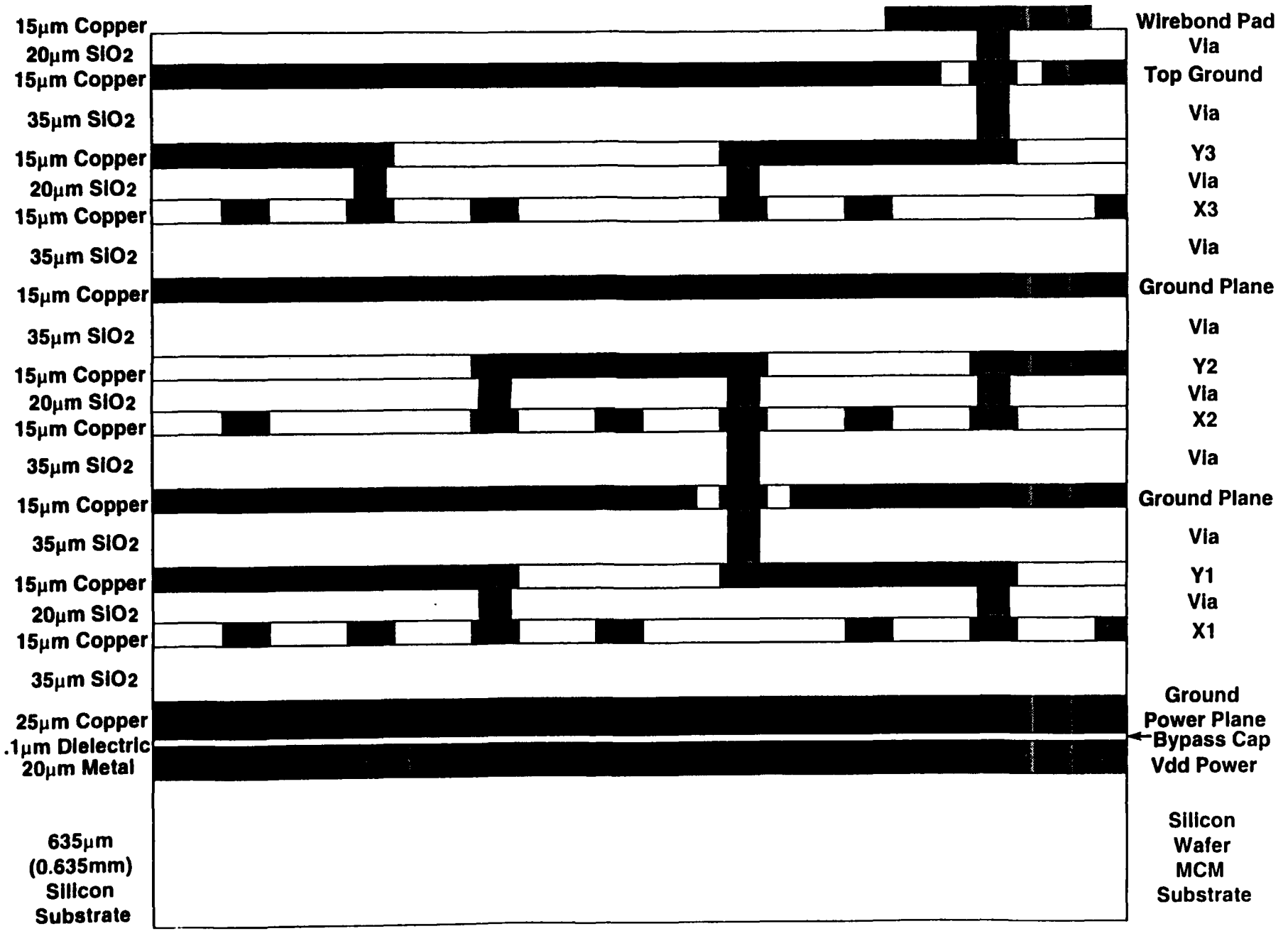


Figure 2

'Silicon Circuit Board' Conventional MCM With Two Signal Interconnect Layers

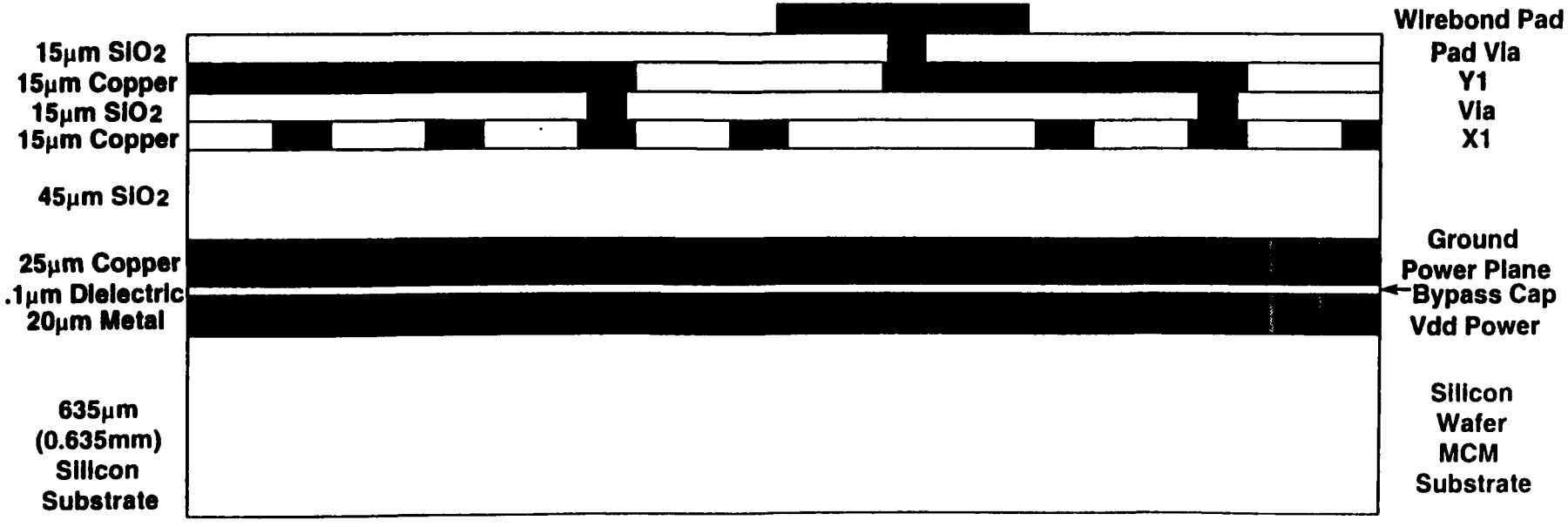


Figure 3

performance. (In principle, however, sharply reducing the required total MCM area and the number of MCMs [typically to only one], and largely eliminating a whole level of packaging, should be capable of sharply reducing system costs [offset to some degree by the cost of cryogenic cooling]). In fact, however, suitably designed IC chips have much shorter logic delays when operated at liquid nitrogen (77°K) temperature than when operated at room temperature (2X to 3X faster for CMOS is frequently cited). Hence, by shortening both the logic delay (which taken by itself would not be too effective if the interconnect delay were not changed) and at the same time reducing the interconnect delay (by mounting everything on a single maximal density MCM), adoption of the HTSC MCM approach could lead to up to 3X speed improvements at the system level. Remembering that if the speed of a $1M machine is increased 3X it is worth at least $3M (sometimes much more than that), it would appear that there is plenty of value margin to pay for the cost and inconvenience of having to do cryogenic cooling.

1.4 HTSC/Cu MCM Comparisons vs. Signal Risetime/Frequency and Extension to 77°K Cu and Self-Termination Cases Favorable for Cu

It is important to remember that the reason for the attractiveness of HTSC MCM packaging in terms of system performance, low cost, small size, etc., has nothing to do with the interconnects being superconducting per se. It is just the fact that the chips operate faster at 80°K and that the use of HTSC interconnects allows all of them to be placed essentially shoulder to shoulder on a single very large, very high density MCM which, because only 2 signal layers are required, should be reasonably easy to manufacture, test and repair. If by some means it were possible to invent some other new technology or combination of technologies which could duplicate this same MCM size and density (and also operate at cryogenic temperatures) and also be manufacturable, testable and repairable, then it could serve as well. Of course, these alternatives may themselves be more difficult to develop than HTSC MCMs, or have other disadvantages, but they are worth considering.

The first alternative would be copper interconnects cooled to 80°K. For pulse rise times in the 40ps to 0.4ns range, the maximum signal frequency components are in the 10^9 to 10^{10} Hz range. While room temperature copper ($\rho = 1.70\,\mu\,\Omega$-cm) has a surface resistance, R_{surf} of 8.3 mΩ at 10^9 Hz or 26 mΩ at 10^{10} Hz, when copper wire is cooled to 77°K, R_{surf} falls to about 3.9 mΩ at 10^9 Hz or 14 mΩ at 10^{10} Hz, about a factor of 2 improvement (these are measured R_{surf} values from Ref. 5, not simply scaled from the $\approx$ 5 x reduction in resistivity from 300°K to 77°K). Assuming that the conductor thickness, t_w, is well over twice the skin depth, to keep the series resistance of a wire of width W and length L to some maximum value, R_{max}, we must have

$$R_{max} \approx \frac{L}{2W} R_{surf} \qquad \text{Eq. 4}$$

This expression ignores the sidewall contribution to conduction, by taking as the wire periphery 2W instead of the actual periphery of $2(W + t_w) = 3W$ for a wire thickness of $t_w = W/2$. This is offset by the fact that we have ignored the effect of the nonuniform current distribution on the wire and the resistance in the ground plane which increases the ac resistance. Eq. 4 is essentially equivalent here to assuming a current form factor of 2/3 in calculating skin effect line loss, and should be reasonably accurate. From Eq. 4, the minimum allowable linewidth, W_{min}, necessary to keep the resistance of a line of length L_{max} lower than R_{max} is given by

$$W_{min} \approx \frac{L_{max} R_{surf}}{2 R_{max}} \qquad \text{Eq. 5}$$

For example, for a 6" MCM with L_{max} = 12" and taking $R_{max} = 10\,\Omega$, W_{MIN} for 77°K copper would be $W_{min} = 59.4\,\mu$m (2.34 mils) at 10^9 Hz or $W_{min} = 213\,\mu$m (8.4 mils) at 10^{10} Hz.

To quantitatively evaluate the effect of cryogenic cooling of copper interconnects and other options on the comparison between HTSC and Cu MCMs, we will treat one specific case under the various conditions. Let us consider a maximal-density

MCM fabricated from 10K-gate VLSI chips, 0.6 cm square, flip-chip mounted on 0.635 cm centers in a square array (as in Fig.1), with 370 I/O pads per die (from the high performance chip Rent's rule curve of Ref.2, Pg. 14, Fig. 1-7). Table 1 presents the calculation results of the number, S, of 300°K copper interconnect layers required to complete the inter-chip wiring with an $R_{max} = 10\Omega$ maximum line resistance, as compared to the number of W = 1.5m HTSC layers required as the number of rows and columns is increased from NR = 2 to 40 (NC = 4 to 1600 total die), corresponding to MCM sizes (edge dimensions) from XM = 0.5 inches to 10 inches. Note that the calculational details on Tables 1 - 4 such as copper skin depth, R_{surf}, and required signal linewidth, W (called XW in Tables 1 - 4) are for a signal frequency of 1GHz (or pulse risetime of about 400ps) only, but the number of signal layers, S, required for dc or other frequency/risetime values have been added as well. Use Eq. 3 to calculate linewidth, W, values corresponding to other frequency points from the values of S at the desired frequency and R_{bar} (which is a function of size only) from the tables.

The calculated number of 300°K copper signal layers, S, for $R_{max} = 10\Omega$ is plotted against MCM size, XM (in inches) for dc and signal frequency components of 300MHz, 1GHz, 3GHz, 10GHz and 30GHz in Fig. 4. Using the usual signal risetime, Tr, vs signal bandwidth, f, relationship of f = 0.4/Tr (0.36 from the Fourier transform of a Gaussian pulse, for example), these frequencies correspond respectively to risetimes of about 1.3ns (eg., 300°K CMOS), 400ps (eg., 77°K CMOS), 130ps (300°K GaAs or fast ECL), 40ps (eg., 77°K GaAs HEMT or Si-Ge ECL) and 13ps (eg., advanced 77°K GaAs HBT). Inasmuch as 15 GHz room temperature performance with 26 ps to 34 ps (unloaded/loaded) gate delays in 500-gate gate arrays has already been demonstrated (using GaAs HBTs with over 55 GHz f_t and f_{max} values), even the 30GHz frequency is within the range which will have to be considered for some late 90's MCM applications. We note in Fig. 4 that room temperature copper is essentially useless in this frequency range, requiring, for $R_{max} = 10\Omega$, over 22 signal layers just to interconnect 4 die in a 0.5" MCM. Probably the lowest risetime of broad interest for mid to late 90's ICs will be about 0.4 ns, corresponding to 1GHz frequencies. At 1GHz it would take 94 layers of 300°K copper signal interconnects to wire a 4" MCM with 256 10K-gate chips on it

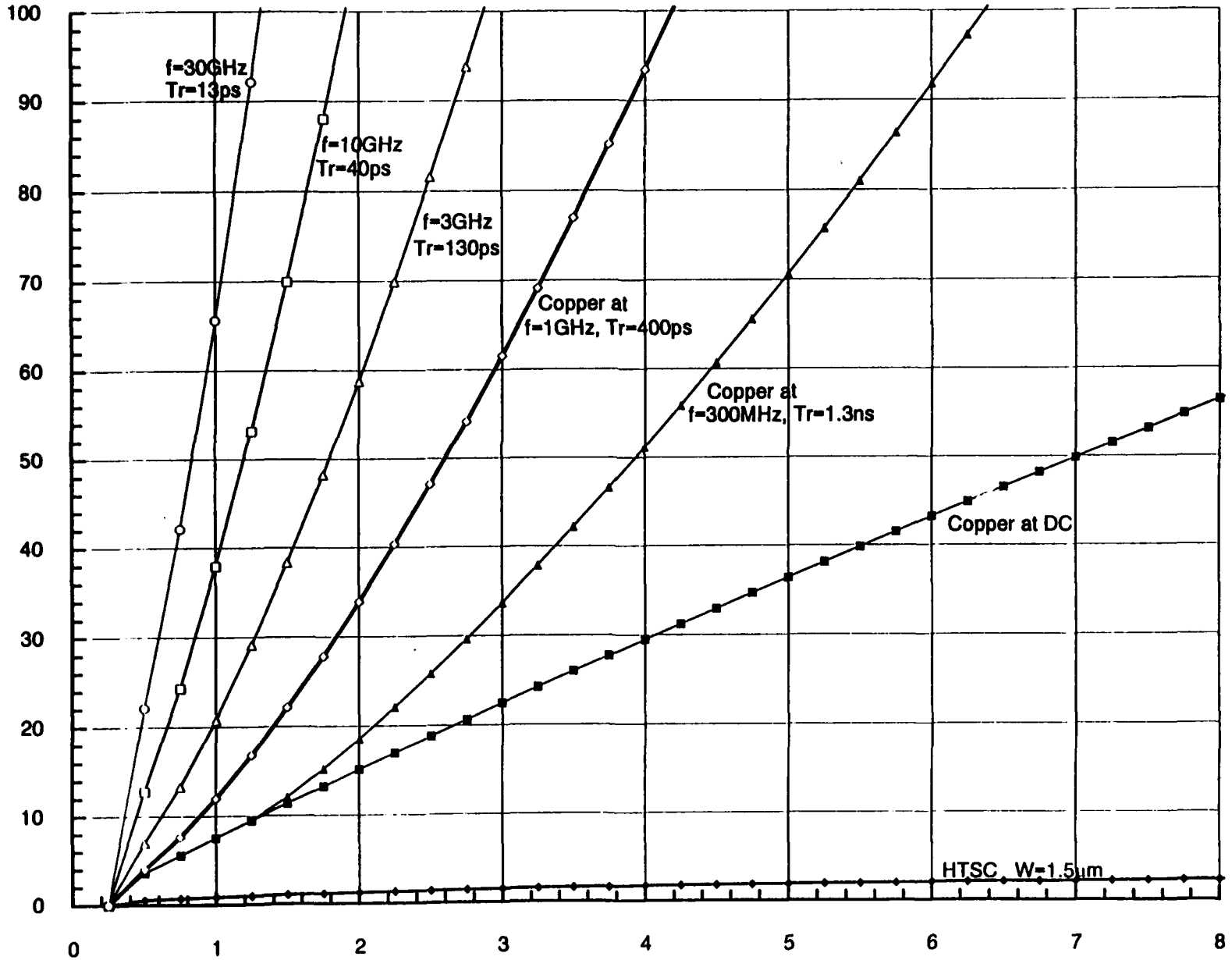
Rmax=10Ω 10K-Gate Flip-Chip Max-Density MCM Comparison of HTSC with 300°K Copper at Various Frequencies

300°K Copper for Rmax=10.0Ω at Various Frequencies Summary Chart R. C. Eden January 1992
AC (Skin Effect) Calculation at Freq= 1000 MHz
10K-gate Flip-Chip Rmax= 10 .0Ω vs. HTSC with W= 1.500 μm Linewidth.
Comparison of # Signal Layers Req'd on MCM for HTSC vs. Donath's theory and Rent's rule p
Array assumed square with NR rows and NR Columns and NC=NR^2 Chips
Data Below for 300°K Copper at f=1GHz
Skin Depth, DELTA= 2.075127E-04 cm, Current Distribution Form Factor taken as FF= 1 (actually 2/3 as sidewall conduction discounted)
The Rent's Rule exponent assumed in this calculation is p= .6666667
10K-gate Flip-Chip of Xc= .8 cm square with Xg= .035 cm gaps between chips for a Xp= .8350 cm mounting pitch.
IOP= 370 I/O Pads per chip
Pn= 2 (# Pad conns. per wire), Weff= .4000 (wiring efficiency), and signal line pitch to W ratio= 4
Conductor resistivity= 1.70E-06 ohm-cm, with thickness to width ratio of WTR= 0.5
NC is the total number of chips on the MCM (=NR^2) and Rbar is the average wire length (in pitches)
XM is the overall size of the square MCM in cm, and S is the # sig layers req'd to keep R of a 2*XM line <Rmax
Rmax= 10 ohms Maximum Line Resistance Allowed for Longest (L=2*XM) Line.

				f=1.0GHz	f=1.0GHz		All Frequencies					
NR=	NC=	Rbar=	XM (cm)	XW (cm)	S (# w copper)	Xm (inches)	S w HTSC lines	Copper at dc	Cu at f=300MHz	Cu at f=1GHz	Cu at f=3GHz	Cu at f=10Ghz	Cu at f=30Ghz
1	1	0	0.635	0	0	0.25	0	0	0	0	0	0	0
2	4	1.333333	1.27	0.00104	4.041521	0.5	0.5826772	3.609882	3.609882	4.041521	7.000119	12.78041	22.13632
3	9	1.692043	1.905	0.00156	7.693231	0.75	0.7394362	5.610627	5.610627	7.693231	13.32507	24.32813	42.13756
4	16	1.97748	2.54	0.00208	11.98604	1	0.8641745	7.571492	7.571492	11.98604	20.7639	37.90952	65.66121
5	25	2.219543	3.175	0.0026	16.81937	1.25	0.9699579	9.501408	9.501408	16.81937	29.132	53.18752	92.12348
6	36	2.432199	3.81	0.00312	22.11701	1.5	1.06289	11.40549	12.11399	22.11701	38.30779	69.94014	121.1399
7	49	2.623289	4.445	0.00364	27.83045	1.75	1.146398	13.28723	15.24336	27.83045	48.20375	88.00761	152.4336
8	64	2.797724	5.08	0.00416	33.92118	2	1.222628	15.14918	18.5794	33.92118	58.75321	107.2682	185.794
9	81	2.956821	5.715	0.00468	40.35871	2.25	1.293028	16.99336	22.10538	40.35871	69.90334	127.6254	221.0538
10	100	3.106937	6.35	0.0052	47.11812	2.5	1.35863	18.82137	25.80766	47.11812	81.61098	149.0006	258.0766
11	121	3.24982	6.985	0.00572	54.17863	2.75	1.420197	20.63455	29.67486	54.17863	93.84013	171.3279	296.7486
12	144	3.382805	7.62	0.00624	61.52254	3	1.478312	22.43401	33.69728	61.52254	106.5602	194.5514	336.9728
13	169	3.508941	8.255	0.00676	69.13461	3.25	1.533435	24.22072	37.86658	69.13461	119.7447	218.6228	378.6658
14	196	3.629068	8.89	0.00728	77.0015	3.5	1.585931	25.99551	42.17545	77.0015	133.3705	243.5001	421.7545
15	225	3.743669	9.525001	0.0078	85.11143	3.75000039	1.6361	27.75911	46.61745	85.11143	147.4173	269.146	466.1745
16	256	3.85391	10.16	0.00832	93.45395	4	1.684189	29.51216	51.18684	93.45395	161.867	295.5273	511.8684
17	289	3.959668	10.795	0.00884	102.0196	4.25	1.730408	31.25522	55.87846	102.0196	176.7032	322.6144	558.7846
18	324	4.061544	11.43	0.00936	110.8	4.5	1.774927	32.98882	60.68766	110.8	191.9112	350.3804	606.8766
19	361	4.159884	12.065	0.00988	119.7873	4.75	1.817902	34.71342	65.61022	119.7873	207.4777	378.8008	656.1022
20	400	4.254985	12.7	0.0104	128.9746	5	1.859462	36.42942	70.64227	128.9746	223.3905	407.8534	706.4227
21	441	4.347108	13.335	0.0109	138.3552	5.25	1.899719	38.13723	75.78027	138.3552	239.6383	437.5176	757.8027
22	484	4.436474	13.97	0.0114446	147.9233	5.5	1.938774	39.83718	81.02094	147.9233	256.2107	467.7746	810.2094
23	529	4.52329	14.605	0.012	157.6734	5.75	1.976713	41.52959	86.36126	157.6734	273.0983	498.607	863.6126
24	576	4.607732	15.24	0.0125	167.6002	6	2.013615	43.21477	91.79842	167.6002	290.2921	529.9984	917.9841
25	625	4.68996	15.875	0.013	177.6991	6.25	2.049549	44.89297	97.32979	177.6991	307.7838	561.9338	973.2979
26	676	4.770113	16.51	0.0135	187.9655	6.5	2.084577	46.56447	102.9529	187.9655	325.5658	594.399	1029.529
27	729	4.848322	17.145	0.014	198.3953	6.75	2.118755	48.22949	108.6656	198.3953	343.6307	627.3809	1086.656
28	784	4.924702	17.78	0.0146	208.9845	7	2.152134	49.88825	114.4655	208.9845	361.9718	660.867	1144.655
29	841	4.999358	18.415	0.0151	219.7295	7.25	2.184759	51.54096	120.3508	219.7295	380.5826	694.8455	1203.508
30	900	5.072385	19.05	0.0156	230.6267	7.5	2.216672	53.18782	126.3194	230.6267	399.4571	729.3055	1263.194
31	961	5.143871	19.685	0.0161	241.6728	7.75	2.247912	54.82899	132.3697	241.6728	418.5896	764.2366	1323.697
32	1024	5.213896	20.32	0.0166467	252.8648	8	2.278514	56.46465	138.4998	252.8648	437.9747	799.6287	1384.998
33	1089	5.282534	20.955	0.0172	264.1996	8.25	2.308509	58.09497	144.7081	264.1996	457.6072	835.4727	1447.081
34	1156	5.349851	21.59	0.0177	275.6745	8.5	2.337927	59.72009	150.9932	275.6745	477.4823	871.7595	1509.932
35	1225	5.415912	22.225	0.0182	287.2868	8.75	2.366796	61.34016	157.3535	287.2868	497.5953	908.4806	1573.535
36	1296	5.480772	22.86	0.0187	299.0338	9	2.395141	62.95531	163.7876	299.0338	517.9418	945.628	1637.876
37	1369	5.544488	23.495	0.0192	310.9132	9.25	2.422985	64.56567	170.2942	310.9132	538.5176	983.194	1702.942
38	1444	5.607108	24.13	0.0198	322.9227	9.5	2.450351	66.17136	176.8721	322.9227	559.3185	1021.171	1768.721
39	1521	5.668679	24.765	0.0203	335.06	9.75	2.477257	67.7725	183.5199	335.06	580.3409	1059.553	1835.199
40	1600	5.729245	25.4	0.0208	347.3229	10	2.503725	69.3692	190.2366	347.3229	601.5809	1098.331	1902.366

Table 1

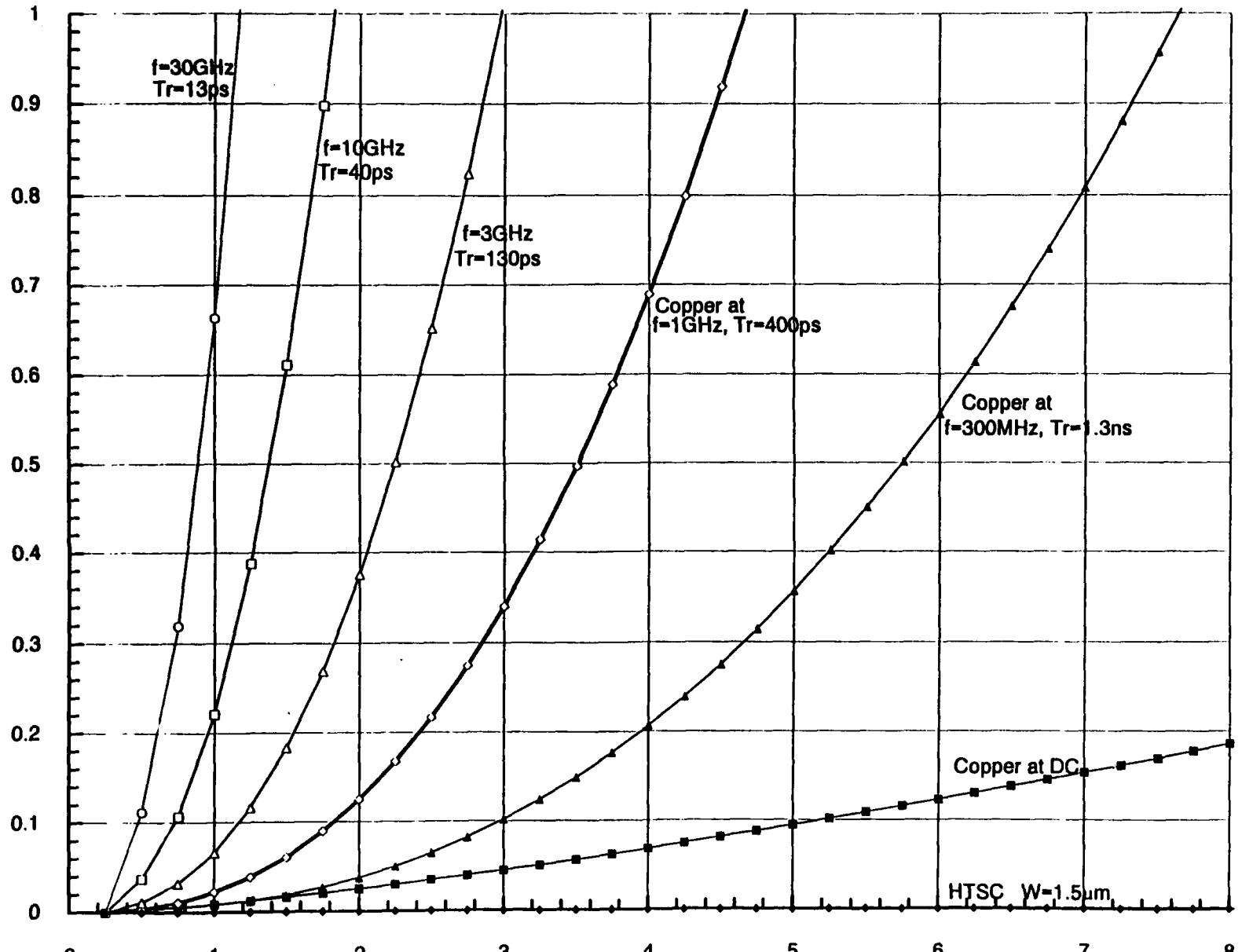
Rmax=10Ω 10K-Gate (370 I/O) Flip-Chip Max-Density MCM Comparison of HTSC to 300°K Copper Interconnects vs. Frequency



Horizontal is Edge Size of MCM in inches, Vertical is Number of Signal Layers Required to Complete Inter-Chip Wiring

Figure 4

Tmat for Rmax=10Ω 10K-Gate (370 I/O) Flip-Chip Max-Density MCM Comparison of HTSC to 300°K Copper vs. Frequency



Horizontal is Edge Size of MCM in inches, Vertical is Thickness of Wiring Mat in inches for Zo=50Ω, Er=3.9 Dielectric

Figure 5

(or 142 total metal layers including grounds), as compared to 2 layers of W = 1.8μm HTSC interconnects. Note that in a typical "triplate" (as shown for S = 6 in Fig. 2) configuration, the total thickness of the interconnect mat for S layers of linewidth W will be of the order of

$$t_{mat} = 2.25SW \qquad \text{Eq. 6}$$

where the constant 2.25 is appropriate for $\varepsilon_r = 3.9$ with $Z_o = 50\Omega$ as seen in Fig. 2. Hence, noting in Table 1 for this S = 94 case, W = 83μm, so the total wiring mat thickness would be an incredible 0.7 inches (a thickness of 17% of the 4" size of the MCM)! As shown in the plot of t_{mat} versus X_M for various frequencies in Fig. 5, the situation is so far out of hand for larger MCM sizes or higher signal frequencies that the use of 300°K copper is not worth discussing there.

As noted above, cryogenically cooling the copper can reduce the resistivity by nearly 5x which substantially reduces the number of interconnect layers required for a given MCM size or signal frequency or risetime. Table 2 presents results of the calculation for $R_{max} = 10\Omega$ for the maximal density 10K-gate MCM example cited above, when the copper interconnects are cooled to 77°K. Note again that the 77°K skin depth, R_{surf} and W values in Table 2 are for f = 1GHz only; use Eq. 7 for R_{surf} at other frequencies, and Eq. 3 with R_{bar} and S from Table 2 to get signal linewidth, W, values at other frequencies. These $R_{max} = 10\Omega$, 77°K Cu results are plotted in Fig. 6, and the wiring mat thicknesses in Fig.7, for comparison to the HTSC MCM. Note that cooling the copper reduces the number of signal layers for a 4" MCM supporting 0.4ns risetimes (f = 1GHz curve in Fig. 6) from S = 94 at 300°K to S = 44 at 77°K, and reduces the wiring mat thickness from 0.7 inches to a, still thick, but much more reasonable $t_{mat} = 0.156$ inches. For rather slow (probably too slow for cooled CMOS) Tr = 1.3ns signal risetimes (300MHz curve in Fig. 6), the $R_{max} = 10\Omega$ can be met even for an XM = 6" maximal density MCM with S = 44 layers of 77°K Cu (with W = 32.5μm lines for $t_{mat} = 2.25SW = 0.126$ inches). While this 77°K copper represents a significant improvement over 300°K operation, it is a far cry from HTSC, where just 2 signal layers of W = 1.5μm HTSC interconnects would be adequate for a 6" maximal-density MCM, even out to extremely high signal frequencies. Of course,

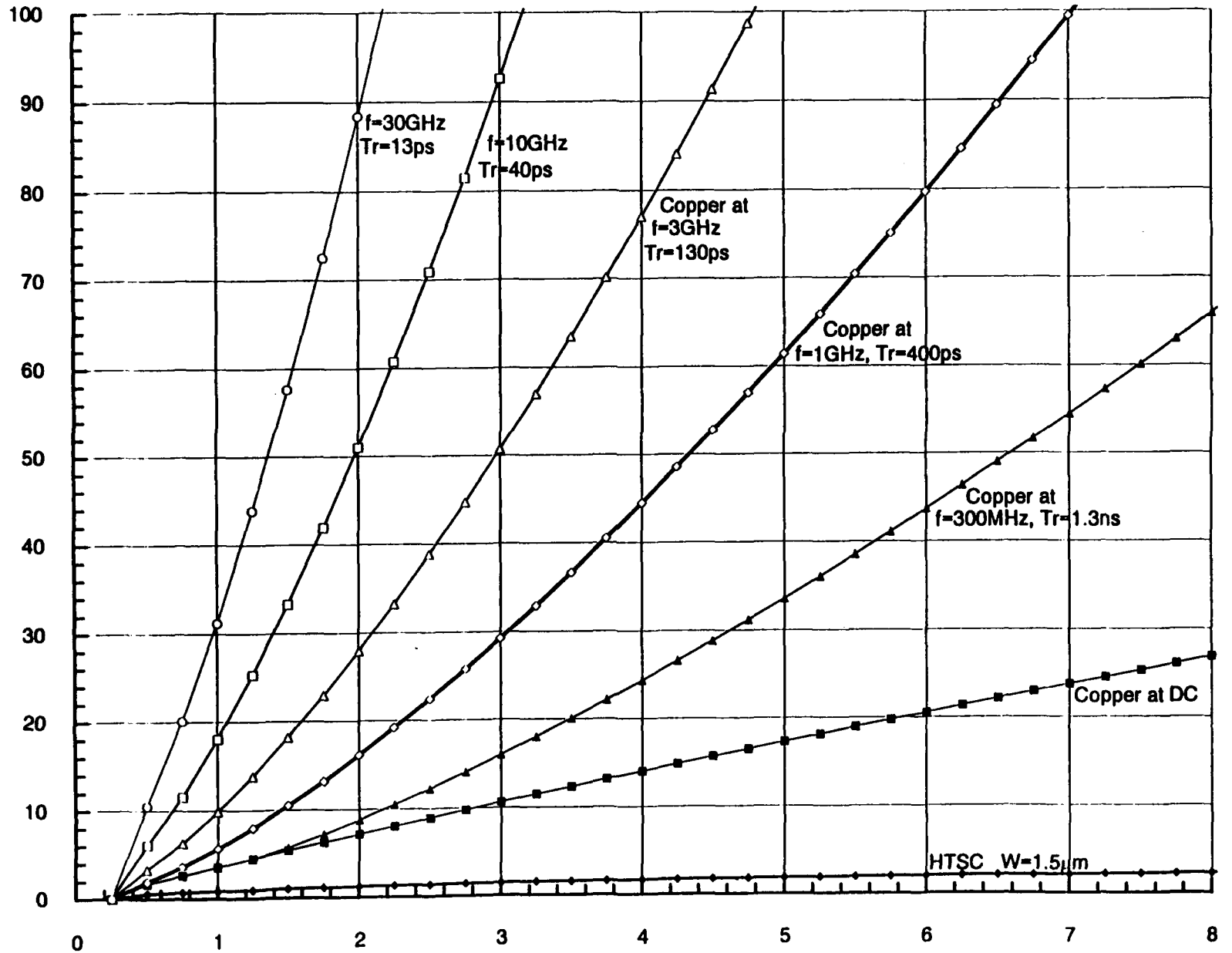
Rmax=10Ω 10K-Gate Flip-Chip Max-Density MCM Comparison of HTSC with 77°K Copper at Various Frequencies

77°K Copper for Rmax=10.0Ω for Various Signal Component Frequencies R. C. Eden January 1992
AC (Skin Effect) Calculation at Freq= 1000 MHz
10K-gate Flip-Chip Rmax= 10.0Ω vs. HTSC with W= 1.500 μm Linewidth.
Comparison of # Signal Layers Req'd on MCM for HTSC vs. Donath's theory and Rent's rule p
Array assumed square with NR rows and NR Columns and NC=NR^2 Chips
Following Data is for T=77°K Coppper at f=1GHz
Skin Depth, DELTA= 9.875305E-05 cm, Current Distribution Form Factor taken as FF= 1 (actually 2/3 as sidewall conduction discounted)
Copper Surface Resistance, Rsurf= 3.898614E-03 Ω
The Rent's Rule exponent assumed in this calculation is p= .6666667
10K-gate Flip-Chip of Xc= 0.6 cm square with Xg= 0.035 cm gaps between chips for a Xp= 0.6350 cm mounting pitch.
IOP= 370 I/O Pads per chip
Pn= 2 (# Pad conns. per wire), Weff= .4000 (wiring efficiency), and signal line pitch to W ratio= 4
Conductor resistivity= .000000385 ohm-cm, with thickness to width ratio of WTR= .5
NC is the total number of chips on the MCM (=NR^2) and Rbar is the average wire length (in pitches)
XM is the overall size of the square MCM in cm, and S is the # sig layers req'd to keep R of a 2*XM line <Rmax
Rmax= 10 ohms Maximum Line Resistance Allowed for Longest (L=2*XM) Line.

NR=	NC=	Rbar=	XM (cm)	f=1GHz XW (cm)	f=1GHz S (# w copper)	All frequencies Xm (inches)	All frequencies S w HTSC lines	Copper at dc	Cu at f=300MHz	Cu at f=1GHz	Cu at f=3GHz	Cu at f=10GHz	Cu at f=30GHz
1	1	0	0.6350001	0	0	0.25	0	0	0	0	0	0	0
2	4	1.333333	1.27	0.000495124	1.923316	0.5	0.5826772	1.717904	1.717904	1.923316	3.331281	6.08206	10.53444
3	9	1.692043	1.905	0.000742686	3.661126	0.75	0.7394362	2.670037	2.670037	3.661126	6.341256	11.5775	20.05281
4	16	1.97748	2.54	0.000990248	5.70498	1	0.8641745	3.603192	3.603192	5.70498	9.881315	18.04073	31.24748
5	25	2.219543	3.175	0.00123781	8.004157	1.25	0.9699579	4.521618	4.521618	8.004157	13.86361	25.31137	43.84058
6	36	2.432199	3.81	0.001485372	10.52525	1.5	1.06289	5.427752	5.764916	10.52525	18.23027	33.28376	57.64917
7	49	2.623289	4.445	0.001732934	13.24421	1.75	1.146396	6.32325	7.254153	13.24421	22.93965	41.88187	72.54153
8	64	2.797724	5.08	0.001980496	16.14273	2	1.222628	7.209334	8.841736	16.14273	27.96002	51.04778	88.41736
9	81	2.958821	5.715	0.002228058	19.20628	2.25	1.293028	8.086958	10.51971	19.20628	33.26625	60.73558	105.1971
10	100	3.108937	6.35	0.00247562	22.42301	2.5	1.35863	8.956888	12.28159	22.42301	38.83779	70.90778	122.8159
11	121	3.24982	6.985	0.002723182	25.78303	2.75	1.420197	9.819759	14.12195	25.78303	44.65751	81.53309	141.2195
12	144	3.382805	7.62	0.002970744	29.27792	3	1.478312	10.6761	16.03618	29.27792	50.71084	92.58491	160.3618
13	169	3.508941	8.255	0.003218306	32.90042	3.25	1.533435	11.52638	18.0203	32.90042	56.9852	104.0403	180.203
14	196	3.629068	8.89	0.003465868	36.64418	3.5	1.585931	12.37099	20.07085	36.64418	63.46959	115.8791	200.7085
15	225	3.743869	9.525	0.00371343	40.50362	3.75	1.6361	13.21026	22.18474	40.50362	70.15432	128.0837	221.8474
16	256	3.85391	10.16	0.003960992	44.47373	4	1.684189	14.04452	24.35927	44.47373	77.03076	140.6383	243.5927
17	289	3.959668	10.795	0.004208554	48.55005	4.25	1.730406	14.87402	26.59196	48.55005	84.09116	153.5287	265.9196
18	324	4.061544	11.43	0.004456116	52.72853	4.5	1.774927	15.69903	28.88061	52.72853	91.3285	166.7423	288.8061
19	361	4.159884	12.065	0.004703678	57.0055	4.75	1.817902	16.51974	31.2232	57.0055	98.73643	180.2672	312.232
20	400	4.254985	12.7	0.00495124	61.37761	5	1.859462	17.33637	33.6179	61.37761	106.3091	194.093	336.179
21	441	4.347106	13.335	0.005198802	65.84176	5.25	1.899719	18.1491	36.06301	65.84176	114.0413	208.2099	360.6302
22	484	4.436474	13.97	0.005446364	70.39512	5.5	1.938774	18.95809	38.557	70.39512	121.9279	222.6089	385.5699
23	529	4.52329	14.605	0.005693926	75.03506	5.75	1.976713	19.76349	41.0984	75.03506	129.9645	237.2817	410.9839
24	576	4.607732	15.24	0.005941488	79.75914	6	2.013615	20.56544	43.68588	79.75914	138.1469	252.2205	436.8588
25	625	4.68996	15.875	0.00618905	84.56508	6.25	2.049549	21.36409	46.3182	84.56508	146.471	267.4182	463.182
26	676	4.770113	16.51	0.006436612	89.45075	6.5	2.084577	22.15953	48.9942	89.45075	154.9333	282.8681	489.942
27	729	4.848322	17.145	0.006684174	94.41418	6.75	2.118755	22.9519	51.71278	94.41418	163.5302	298.5638	517.1277
28	784	4.924702	17.78	0.006931736	99.45348	7	2.152134	23.74128	54.47291	99.45348	172.2585	314.4995	544.7291
29	841	4.999358	18.415	0.007179298	104.5669	7.25	2.184759	24.52779	57.27364	104.5669	181.1152	330.6695	572.7365
30	900	5.072385	19.05	0.00742686	109.7528	7.5	2.216672	25.31151	60.11406	109.7528	190.0974	347.0687	601.1406
31	961	5.143871	19.685	0.007674422	115.0095	7.75	2.247912	26.09253	62.9933	115.0095	199.2023	363.692	629.933
32	1024	5.213896	20.32	0.007921983	120.3356	8	2.278514	26.87092	65.91055	120.3356	208.4275	380.5347	659.1055
33	1089	5.282534	20.955	0.008169546	125.7298	8.25	2.308509	27.64677	68.86504	125.7298	217.7704	397.5925	688.6504
34	1156	5.349851	21.59	0.008417108	131.1906	8.5	2.337927	28.42015	71.85603	131.1906	227.2287	414.861	718.5602
35	1225	5.415912	22.225	0.008664669	136.7167	8.75	2.366796	29.19112	74.88282	136.7167	236.8003	432.3362	748.8282
36	1296	5.480772	22.86	0.008912232	142.307	9	2.395141	29.95975	77.94475	142.307	246.4829	450.0142	779.4475
37	1369	5.544488	23.495	0.009159794	147.9603	9.25	2.422985	30.72611	81.04118	147.9603	256.2747	467.8915	810.4119
38	1444	5.607108	24.13	0.009407355	153.6754	9.5	2.450351	31.49024	84.17151	153.6754	266.1737	485.9644	841.715
39	1521	5.668679	24.765	0.009654918	159.4514	9.75	2.477257	32.2522	87.33515	159.4514	276.178	504.2297	873.3515
40	1600	5.729245	25.4	0.00990248	165.2872	10	2.503725	33.01206	90.53155	165.2872	286.2859	522.6841	905.3155

Table 2

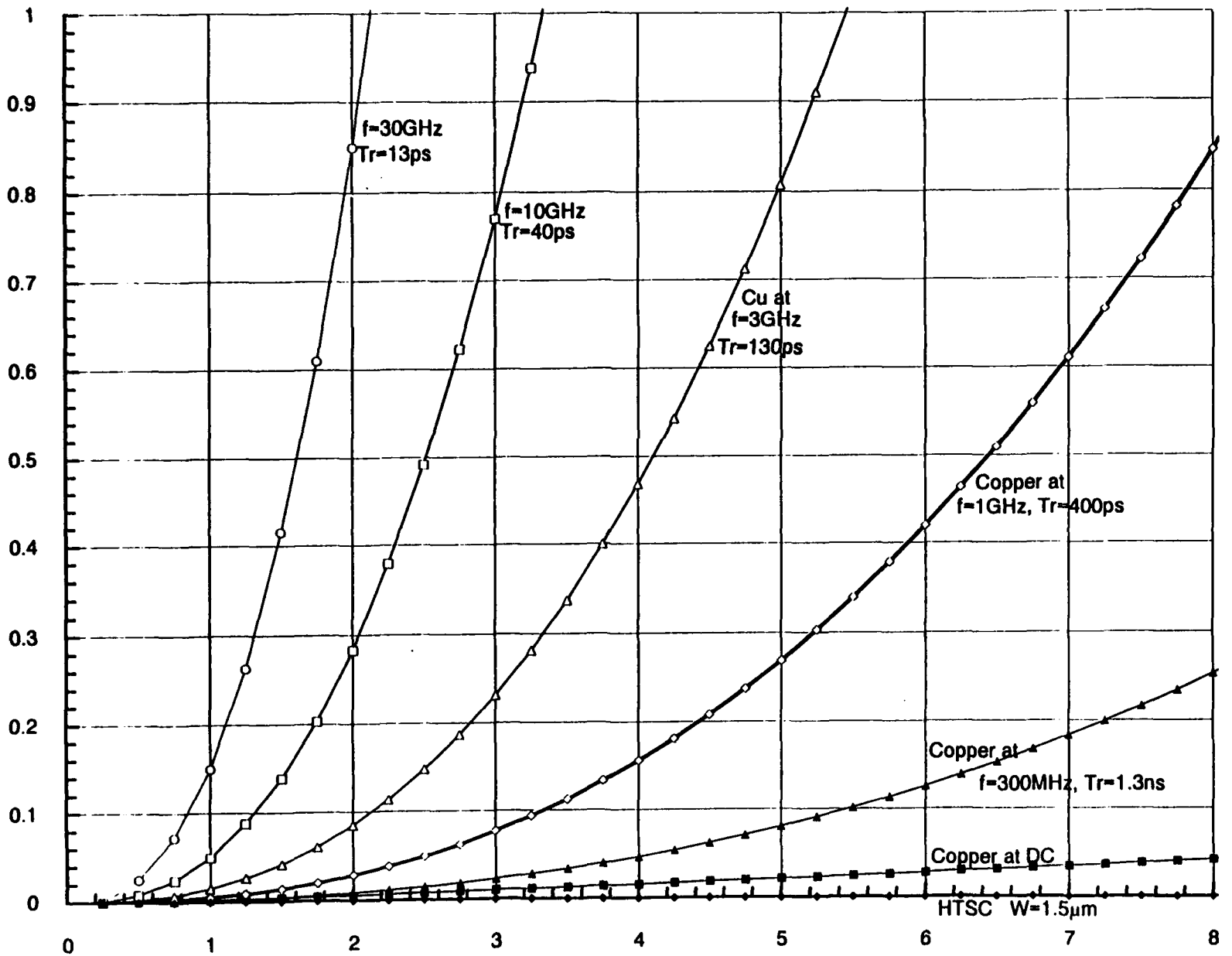
Rmax=10Ω 10K-Gate (370 I/O) Flip-Chip Max-Density MCM Comparison of HTSC to 77°K Copper Interconnects vs. Frequency



Horizontal is Edge Size of MCM in inches, Vertical is Number of Signal Layers Required to Complete Inter-Chip Wiring

Figure 6

Tmat for Rmax=10Ω 10K-Gate (370 I/O) Flip-Chip Max-Density MCM Comparison of HTSC to 77°K Copper vs. Frequency



Horizontal is Edge Size of MCM in inches, Vertical is Thickness of Wiring Mat in inches for Zo=50Ω, Er=3.9 Dielectric

Figure 7

while at least the wiring mat thicknesses for 77°K Cu are reasonable, fabricating an S=44 signal layer (67 total metal planes including power/ground planes) with any reasonable yield without some extremely effective repair/rework scheme (very difficult with 67 layers!) seems extremely difficult. (If that is not obvious, just note how complex the S = 6 case in Fig. 2 looks, and imagine what an order of magnitude more layers would be like!) It should also be noted that no one, in my awareness, has demonstrated that a "conventional" copper polyimide, (for example), MCM with so many layers will be reliable in temperature cycling to 77°K.

The signal layer requirements and their dependencies shown above can be understood more clearly with a bit of analysis. For a maximum line length of L_{max}, and assuming a line thickness, t_w, of half of the width, W, with a normal metal resistivity, ρ, the minimum acceptable width to achieve an end to end dc resistance of R_{max} will be given by

$$W = \sqrt{2\rho L_{max}/R_{max}} \qquad \text{Eq. 7}$$

We note, for example, that the minimum acceptable line width, W, varies as the square root of resistivity, ρ, which is the same ρ dependence as obtained for the high frequency skin effect case of Eq. 5, due to the dependency of R_{surf} in Eqs. 1 and 2 on ρ, given by

$$R_{surf} = \sqrt{\pi \rho \mu_0 f} \qquad \text{Eq. 8}$$

where $\mu_0 = 4\pi \times 10^{-9}$ in centimeter units (this equation ignores the complication of anomalous skin effect which alters the low temperature R_{surf} somewhat). In either case, cooling copper from 300°K to 77°K allows a bit over 2x reduction in W and hence 2x reduction in the number of signal layers, as was shown above.

While the dependencies of line width and required number of signal layers on metal resistivity happens to be the same for the "dc" and "ac" (fully developed skin effect conduction) cases, this is not the case for their dependencies on R_{max} or L_{max}, which

tend to be square root in nature for the "dc" case or proportional for the "ac" case. Note that in both the 300°K and 77°K plots, in Figs. 4 and 6, of the required number of signal layers versus MCM size for $R_{max} = 10\Omega$, above an MCM size of 1.2", the 300MHz ac (skin effect limited) curve rises above the "dc-only" curve. The point at which these depart (crossover between dc and fully developed skin effect curves) occurs at a length, L_{eq}, obtained by equating Eqs. 2 and 3 for W, and substituting Eq. 8 for R_{surf} as

$$L_{eq} \approx \frac{8\,R_{max}}{\pi \mu_O f} \qquad \text{Eq. 9}$$

where as usual, f is the frequency of the highest frequency components. L_{eq} here is interpreted as the approximate maximum length for which a R_{max} resistance line can be considered to be dc resistance dominated subject to the above geometric assumptions. From Eq. 9, for $R_{max} = 10\Omega$ and $f = 300MHz$ ($\mu_o = 1.2566E\text{-}8$ Webers/cm ampere), L_{eq} should be 6.75 cm (2.66"), and since the longest line for an MCM of size X_M is $L = 2X_M$, this corresponds to an MCM size of $X_M = L_{eq}/2 = 1.33"$ as seen in Figs. 4 and 6. Taking a more realistic $f = 10^9$ Hz, as appropriate for Tr = 0.4ns logic, the "ac" curve pulls away from the "dc-only" curve for $R_{max} = 10\Omega$ above wire lengths of only 2 cm, and the number of required layers for a 6" MCM at 300°K is S = 178 signal layers (268 total) for $R_{max} = 10\Omega$, or S = 80 signal layers (121 total) if the copper temperature is reduced to 77°K. For really fast logic (eg. GaAs or Si-Ge ECL in the late 90's), $T_R = 40$ ps or $f = 10^{10}$ Hz needs to be considered. Here, cooled copper (Table 2) would require 252 signal layers (379 total) to achieve $R_{max} = 10\Omega$ at 10GHz in the 12" lines for maximal density 6" MCMs. These are, of course, hopelessly large numbers requiring impractically thick "wiring mats", even if it were conceivable to yield them somehow (see Fig. 7). Hence, for higher performance logic with higher signal frequencies, copper has very serious problems in attempting to implement maximal density large MCMs.

A potential source of a significant reduction in the number of normal metal (eg., 77°K copper) signal interconnect layers required would be to alter the chip to chip electrical interconnection scheme in such a way as to increase the allowable maximum line resistance, R_{max}. If R_{max} can be increased by some factor, then for skin-effect dominated frequencies, the number of layers can be proportionately reduced (but never below the dc resistance limit, of course). When the dc resistance is the limitation, the number of signal layers required will drop as the reciprocal of the square root of R_{max}. The value of $R_{max} = 10\ \Omega$ was obtained, as described in more detail in Ref. 1, Section 3.1, as the point for $Z_o = 50\ \Omega$, where dc noise margin in an internal - reference, ECL-type (load terminated, as also used in GaAs) interconnection approach begins to be significantly compromised, and which gives a comparatively small loss in the leading edge amplitudes in source - terminated, open circuit load (CMOS - type) interconnect approaches. For the latter case, it is well known that if the source resistance is correspondingly reduced, a higher line resistance can be tolerated, even up to $R_{line} = Z_o$ for $R_{source} = 0$ if load capacitance effects are ignored. For this ideal case of $R_{max} = 50\Omega$ instead of $R_{max} = 10\ \Omega$, it would take substantially fewer numbers of signal layers to wire the MCM. While in fact there are serious problems with this approach, it is worth examining the implications for MCM wireability anyway. Because the IC driver output impedance tends to be nonlinear, and, of course, is non-zero, a realistic expectation might be that the line ohmic resistance might be able to be increased, for $Z_o = 50\Omega$, to 25Ω (with a combination of IC driver impedance plus source termination resistor also equal to 25Ω) and still maintain fairly good pulse reflection characteristics. This $R_{max} = 25\Omega$ ohmic line resistance should also be useable with load terminated lines if a differential signal configuration were used (although this would increase by 2x the number of wires needed).

This $R_{max} = 25\Omega$ case is treated in Tables 3 and 4 and Figures 8 and 10 for S, and 9 and 11 for t_{mat}. Table 3 and Figure 8 show the results of the calculation of the number of room temperature copper layers, while Table 4 and Figure 10 show the results for 77°K cryogenically cooled copper interconnects. From Eq. 9, we calculate for $R_{max} = 25\Omega$ a 300MHz ac value for L_{eq} of 16.9 cm (6.65", corresponding to an X_M = 3.324" MCM size), or at a more practical 1GHz signal frequency (0.4ns pulse

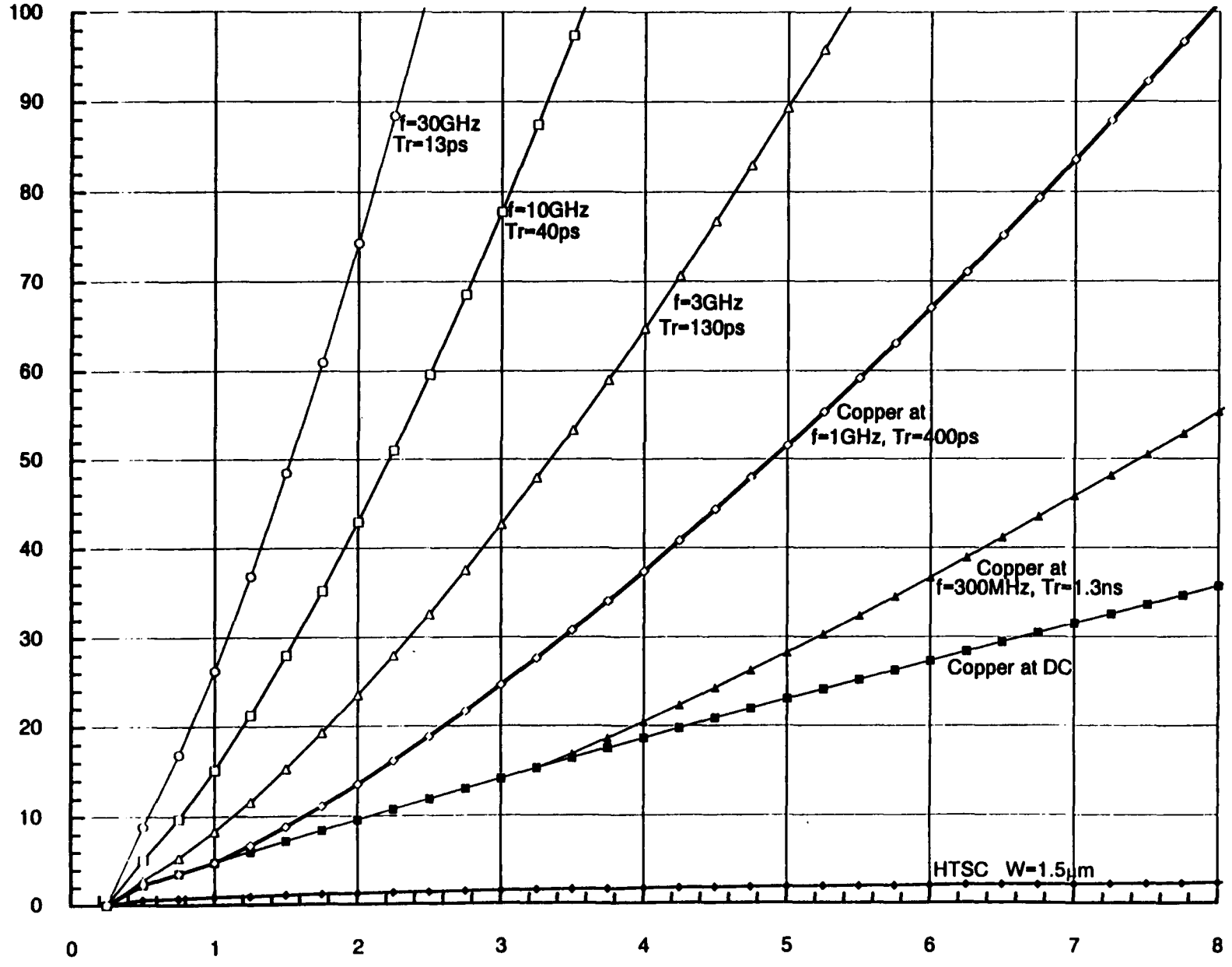
Rmax=25Ω 10K-Gate Flip-Ckip MCM Comparison of HTSC with 300°K Copper at Various Frequencies

300°K Copper for Rmax=25.0Ω for Various Signal Component Frequencies R. C. Eden January 1992
AC (Skin Effect) Calculation at Freq= 1000 MHz
10K-gate Flip-Chip Rmax= 25.0Ω vs. HTSC with W= 1.500 μm Linewidth.
Comparison of # Signal Layers Req'd on MCM for HTSC vs. Donath's theory and Rent's rule p
Array assumed square with NR rows and NR Columns and NC=NR^2 Chips
Data below is for 300°K Copper at f=1GHz
Skin Depth, DELTA= 2.075127E-04 cm, Current Distribution Form Factor taken as FF= 1 (actually 2/3 as sidewall conduction discounted)
The Rent's Rule exponent assumed in this calculation is p= .6666667
10K-gate Flip-Chip of Xc= 0.6 cm square with Xg= 0.035 cm gaps between chips for a Xp= 0.6350 cm mounting pitch.
IOP= 370 I/O Pads per chip
Pn= 2 (# Pad conns. per wire), Weff= .4000 (wiring efficiency), and signal line pitch to W ratio= 4
Conductor resistivity= 1.70E-06 ohm-cm, with thickness to width ratio of WTR= .5
NC is the total number of chips on the MCM (=NR^2) and Rbar is the average wire length (in pitches)
XM is the overall size of the square MCM in cm, and S is the # sig layers req'd to keep R of a 2*XM line <Rmax
Rmax= 25 ohms Maximum Line Resistance Allowed for Longest (L=2*XM) Line.

NR=	NC=	Rbar=	XM (cm)	f=1.0GHz XW (cm)	f=1.0GHz S (# w copper)	All frequencies Xm (inches)	All frequencies S w HTSC lines	Cu at dc	Cu at f=300MHz	Cu at f=1GHz	Cu at f=3GHz	Cu at f=10GHz	Cu at f=30Ghz
1	1	0	0.635	0	0	0.25	0	0	0	0	0	0	0
2	4	1.333333	1.27	0.000588	2.28309	0.5	0.5828772	2.28309	2.28309	2.28309	2.800046	5.112164	8.854527
3	9	1.692043	1.905	0.00072	3.548472	0.75	0.7394362	3.548472	3.548472	3.548472	5.330027	9.731253	16.85502
4	16	1.97748	2.54	0.000832	4.795217	1	0.8641745	4.788632	4.788632	4.795217	8.305556	15.16381	26.26448
5	25	2.219543	3.175	0.00104	6.727747	1.25	0.9699579	6.009218	6.009218	6.727747	11.6526	21.27501	36.84939
6	36	2.432199	3.81	0.00125	8.846806	1.5	1.06289	7.213468	7.213468	8.846806	15.32312	27.97606	48.45595
7	49	2.623289	4.445	0.00146	11.13218	1.75	1.146396	8.403582	8.403582	11.13218	19.2815	35.20304	60.97346
8	64	2.797724	5.08	0.00166	13.56847	2	1.222628	9.581185	9.581185	13.56847	23.50129	42.90726	74.31759
9	81	2.956821	5.715	0.00187	16.14348	2.25	1.293028	10.74754	10.74754	16.14348	27.96133	51.05018	88.4215
10	100	3.108937	6.35	0.00208	18.84725	2.5	1.35863	11.90368	11.90368	18.84725	32.64439	59.60023	103.2306
11	121	3.24982	6.985	0.00229	21.67145	2.75	1.420197	13.05043	13.05043	21.67145	37.53606	68.53114	118.6994
12	144	3.382805	7.62	0.0025	24.60902	3	1.478312	14.18851	14.18851	24.60902	42.62407	77.82054	134.7891
13	169	3.508941	8.255	0.00271	27.65384	3.25	1.533435	15.31853	15.31853	27.65384	47.89786	87.44913	151.4663
14	196	3.629068	8.89	0.00291	30.8006	3.5	1.585931	16.44101	16.87018	30.8006	53.3482	97.40004	168.7018
15	225	3.743869	9.525	0.00312	34.04457	3.75	1.6361	17.5564	18.64698	34.04457	58.96693	107.6584	186.4698
16	256	3.85391	10.16	0.00333	37.38158	4	1.684189	18.66512	20.47473	37.38158	64.7468	118.2109	204.7473
17	289	3.959668	10.795	0.00354	40.80785	4.25	1.730406	19.76754	22.35136	40.80785	70.68128	129.0458	223.5138
18	324	4.061544	11.43	0.00375	44.32	4.5	1.774927	20.86396	24.27506	44.32	76.7845	140.1522	242.7507
19	361	4.159684	12.065	0.00395	47.91493	4.75	1.817902	21.95469	26.24409	47.91493	82.9911	151.5203	262.4409
20	400	4.254985	12.7	0.00416	51.58982	5	1.859462	23.03999	28.25691	51.58982	89.35619	163.1413	282.5691
21	441	4.347106	13.335	0.00437	55.34208	5.25	1.899719	24.1201	30.31211	55.34208	95.8553	175.005	303.1211
22	484	4.436474	13.97	0.00458	59.16933	5.5	1.938774	25.19524	32.40837	59.16933	102.4843	187.1098	324.0838
23	529	4.52329	14.605	0.00479	63.06934	5.75	1.976713	26.26562	34.5445	63.06934	109.2393	199.4428	345.445
24	576	4.607732	15.24	0.00499	67.04008	6	2.013615	27.33142	36.71936	67.04008	116.1168	211.9994	367.1937
25	625	4.68996	15.875	0.0052	71.07963	6.25	2.049549	28.39281	38.93192	71.07963	123.1135	224.7735	389.3192
26	676	4.770113	16.51	0.00541	75.1862	6.5	2.084577	29.44996	41.18118	75.1862	130.2263	237.7596	411.8117
27	729	4.848322	17.145	0.00562	79.35811	6.75	2.118755	30.50301	43.46822	79.35811	137.4523	250.9524	434.6823
28	784	4.924702	17.78	0.00583	83.5938	7	2.152134	31.5521	45.78621	83.5938	144.7887	264.3468	457.8621
29	841	4.999358	18.415	0.00603	87.89178	7.25	2.184759	32.59737	48.14031	87.89178	152.233	277.9382	481.4031
30	900	5.072385	19.05	0.00624	92.25066	7.5	2.216672	33.63893	50.52777	92.25066	159.7828	291.7222	505.2777
31	961	5.143871	19.685	0.00645	96.66913	7.75	2.247912	34.6769	52.94786	96.66913	167.4359	305.6946	529.4786
32	1024	5.213896	20.32	0.00666	101.1459	8	2.278514	35.71138	55.39991	101.1459	175.1899	319.8515	553.999
33	1089	5.282534	20.955	0.00687	105.6799	8.25	2.308509	36.74249	57.88324	105.6799	183.0429	334.1891	578.8325
34	1156	5.349851	21.59	0.00707	110.2698	8.5	2.337927	37.7703	60.39727	110.2698	190.9929	348.7038	603.9727
35	1225	5.415912	22.225	0.00728	114.9147	8.75	2.366796	38.79492	62.94138	114.9147	199.0381	363.3922	629.4138
36	1296	5.480772	22.86	0.00749	119.6135	9	2.395141	39.81643	65.51503	119.6135	207.1767	378.2512	655.1503
37	1369	5.544486	23.495	0.0077	124.3653	9.25	2.422985	40.83491	68.11768	124.3653	215.407	393.2776	681.1768
38	1444	5.607108	24.13	0.00791	129.1691	9.5	2.450351	41.85044	70.74882	129.1691	223.7274	408.4685	707.4882
39	1521	5.668679	24.765	0.00812	134.024	9.75	2.477257	42.86309	73.40796	134.024	232.1364	423.8211	734.0797
40	1600	5.729245	25.4	0.00832	138.9292	10	2.503725	43.87293	76.09464	138.9292	240.6324	439.3326	760.9464

Table 3

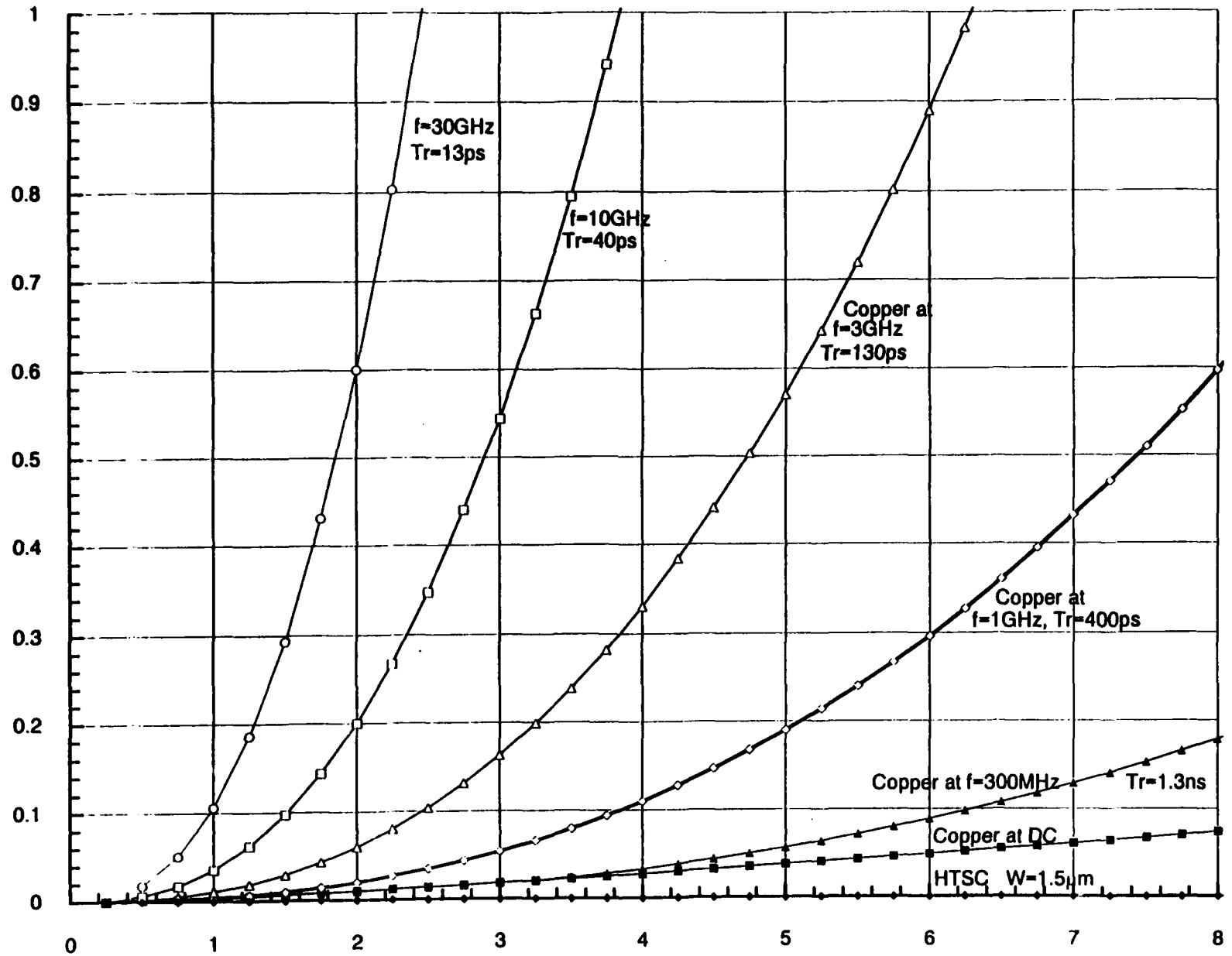
Rmax=25Ω 10K-Gate (370 I/O) Flip-Chip Max-Density MCM Comparison of HTSC to 300°K Copper Interconnects vs. Frequency



Horizontal is Edge Size of MCM in inches, Vertical is Number of Signal Layers Required to Complete Inter-Chip Wiring

Figure 8

Tmat for Rmax=25Ω 10K-Gate (370 I/O) Flip-Chip Max-Density MCM Comparison of HTSC to 300°K Copper vs. Frequency



Horizontal is Edge Size of MCM in inches, Vertical is Thickness of Wiring Mat in inches for Zo=50Ω, Er=3.9 Dielectric

Figure 9

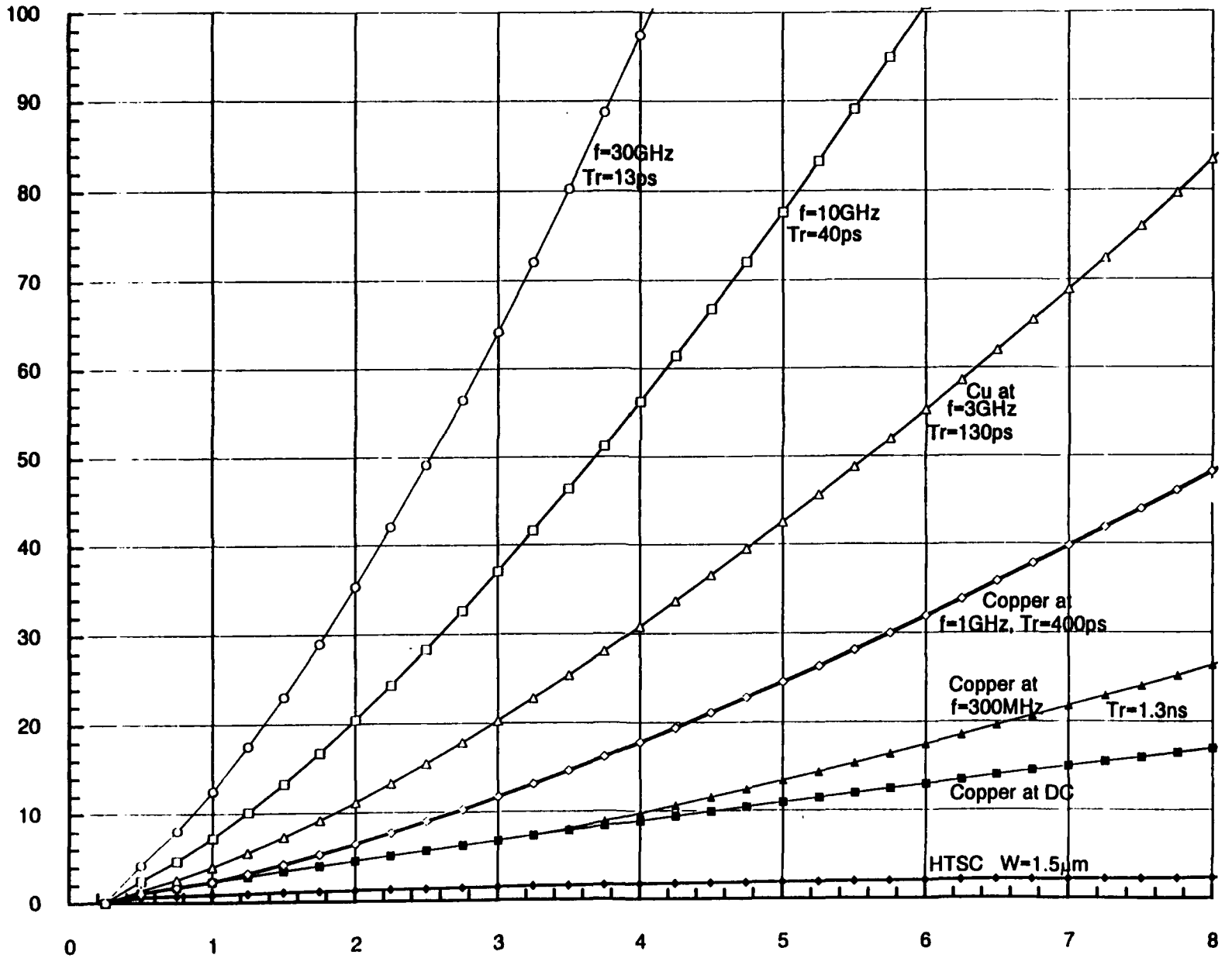
Rmax=25Ω 10K-Gate Flip-Chip Max-Density MCM Comparison of HTSC with 77°K Copper at Various Frequencies

77°K Copper for Rmax=25.0Ω for Various Signal Component Frequencies R. C. Eden January 1992
AC (Skin Effect) Calculation at Freq= 1000 MHz
10K-gate Flip-Chip Rmax= 25.0Ω vs. HTSC with W= 1.500 μm Linewidth.
Comparison of # Signal Layers Req'd on MCM for HTSC vs. Donath's theory and Rent's rule p
Array assumed square with NR rows and NR Columns and NC=NR^2 Chips
Data below for 77°K Copper at f=1GHz
Skin Depth, DELTA= 9.8753045E-05 cm, Current Distribution Form Factor taken as FF= 1 (actually 2/3 as sidewall conduction discounted)
Copper Surface Resistance, Rsurf= 3.898614E-03 Ω at T=77°K, f=1GHz
The Rent's Rule exponent assumed in this calculation is p= .6666667
10K-gate Flip-Chip of Xc= 0.6 cm square with Xg= 0.035 cm gaps between chips for a Xp= 0.6350 cm mounting pitch.
tOP= 370 I/O Pads per chip
Pn= 2 (# Pad conns. per wire), Weff= .4000 (wiring efficiency), and signal line pitch to W ratio= 4
Conductor resistivity= 0.000000385 ohm-cm, with thickness to width ratio of WTR= .5
NC is the total number of chips on the MCM (=NR^2) and Rbar is the average wire length (in pitches)
XM is the overall size of the square MCM in cm, and S is the # sig layers req'd to keep R of a 2*XM line <Rmax
Rmax= 25 ohms Maximum Line Resistance Allowed for Longest (L=2*XM) Line.

				f=1GHz	f=1GHz	All Frequenci	All Frequencies						
NR=	NC=	Rbar=	XM (cm)	XW (cm)	S (# w copper)	Xm (inches)	S w HTSC lines	Copper at dc	Cu at 300MHz	S w Cu at 1GHz	S w Cu at 3GHz	S w Cu at 10GHz	S w Cu at 30GHz
1	1	0	0.635	0	0	0.25	0	0	0	0	0	0	0
2	4	1.333333	1.27	0.0002797	1.086498	0.5	0.5826772	1.086498	1.086498	1.086498	1.332512	2.432824	4.213775
3	9	1.692043	1.905	0.000342561	1.68868	0.75	0.7394362	1.68868	1.68868	1.68868	2.536502	4.630999	8.021125
4	16	1.97748	2.54	0.000398099	2.281992	1	0.8641745	2.278859	2.278859	2.281992	3.952526	7.216292	12.49899
5	25	2.219543	3.175	0.000495124	3.201663	1.25	0.9699579	2.859722	2.859722	3.201663	5.545443	10.12455	17.53623
6	36	2.432199	3.81	0.000594149	4.2101	1.5	1.06289	3.432812	3.432812	4.2101	7.292107	13.3135	23.05967
7	49	2.623289	4.445	0.000693174	5.297685	1.75	1.146396	3.999174	3.999174	5.297685	9.175858	16.75275	29.01661
8	64	2.797724	5.08	0.000792198	6.457091	2	1.222628	4.559583	4.559583	6.457091	11.18401	20.41911	35.36694
9	81	2.958821	5.715	0.000891223	7.68251	2.25	1.293028	5.114641	5.114641	7.68251	13.3065	24.29423	42.07884
10	100	3.108937	6.35	0.000990248	8.969204	2.5	1.35863	5.664834	5.664834	8.969204	15.53512	28.36311	49.12635
11	121	3.24982	6.985	0.001089273	10.31321	2.75	1.420197	6.210561	6.210561	10.31321	17.863	32.61324	56.48779
12	144	3.382805	7.62	0.001188298	11.71117	3	1.478312	6.752162	6.752162	11.71117	20.28434	37.03396	64.14471
13	169	3.508941	8.255	0.001287322	13.16017	3.25	1.533435	7.289924	7.289924	13.16017	22.79408	41.6161	72.08121
14	196	3.629068	8.89	0.001386347	14.65767	3.5	1.585931	7.824098	8.028336	14.65767	25.38783	46.35163	80.28339
15	225	3.743869	9.525001	0.001485372	16.20145	3.75	1.6361	8.354903	8.873898	16.20145	28.06173	51.23347	88.73898
16	256	3.85391	10.16	0.001584397	17.78949	4	1.684189	8.882533	9.743706	17.78949	30.8123	56.25531	97.43707
17	289	3.959668	10.795	0.001683422	19.42002	4.25	1.730406	9.407159	10.63678	19.42002	33.63646	61.4115	106.3678
18	324	4.061544	11.43	0.001782446	21.09141	4.5	1.774927	9.928935	11.55224	21.09141	36.5314	66.69691	115.5224
19	361	4.159884	12.065	0.001881471	22.8022	4.75	1.817902	10.448	12.48928	22.8022	39.49457	72.1069	124.8928
20	400	4.254985	12.7	0.001980496	24.55104	5	1.859462	10.96448	13.44716	24.55104	42.52365	77.63721	134.4716
21	441	4.347106	13.335	0.002079521	26.3367	5.25	1.899719	11.4785	14.42521	26.3367	45.61651	83.26397	144.2521
22	484	4.436474	13.97	0.002178546	28.15805	5.5	1.938774	11.99015	15.4228	28.15805	48.77117	89.04356	154.228
23	529	4.52329	14.605	0.00227757	30.01402	5.75	1.976713	12.49953	16.43936	30.01402	51.98581	94.91268	164.3936
24	576	4.607732	15.24	0.002376595	31.90365	6	2.013615	13.00873	17.47435	31.90365	55.25875	100.8882	174.7435
25	625	4.68996	15.875	0.00247562	33.82603	6.25	2.049549	13.51183	18.52728	33.82603	58.58841	106.9673	185.2728
26	676	4.770113	16.51	0.002574645	35.7803	6.5	2.084577	14.01492	19.59768	35.7803	61.9733	113.1472	195.9768
27	729	4.848322	17.145	0.002673669	37.76567	6.75	2.118755	14.51805	20.68511	37.76567	65.41206	119.4255	206.8511
28	784	4.924702	17.78	0.002772694	39.78139	7	2.152134	15.01531	21.78917	39.78139	68.90339	125.7998	217.8916
29	841	4.999358	18.415	0.002871719	41.82676	7.25	2.184759	15.51274	22.90946	41.82676	72.44607	132.2678	229.0946
30	900	5.072385	19.05	0.002970744	43.9011	7.5	2.216672	16.0084	24.04562	43.9011	76.03894	138.8275	240.4562
31	961	5.143871	19.685	0.003069769	46.0038	7.75	2.247912	16.50236	25.19732	46.0038	79.68092	145.4768	251.9732
32	1024	5.213896	20.32	0.003168794	48.13426	8	2.278514	16.99466	26.36422	48.13426	83.37098	152.2139	263.6422
33	1089	5.282534	20.955	0.003267818	50.29191	8.25	2.308509	17.48535	27.54601	50.29191	87.10815	159.037	275.4601
34	1156	5.349851	21.59	0.003366843	52.47622	8.5	2.337927	17.97448	28.74241	52.47622	90.89148	165.9444	287.4241
35	1225	5.415912	22.225	0.003465868	54.68668	8.75	2.366796	18.46209	29.95313	54.68668	94.72011	172.9345	299.5313
36	1296	5.480772	22.86	0.003564893	56.9228	9	2.395141	18.94821	31.1779	56.9228	98.59318	180.0057	311.779
37	1369	5.544488	23.495	0.003663918	59.18411	9.25	2.422985	19.4329	32.41647	59.18411	102.5099	187.1566	324.1647
38	1444	5.607106	24.13	0.003762942	61.47018	9.5	2.450351	19.91618	33.66861	61.47018	106.4695	194.3858	336.686
39	1521	5.668679	24.765	0.003861967	63.78057	9.75	2.477257	20.39808	34.93406	63.78057	110.4712	201.6919	349.3406
40	1600	5.729245	25.4	0.003960992	66.1149	10	2.503725	20.87866	36.21262	66.1149	114.5144	209.0737	362.1262

Table A

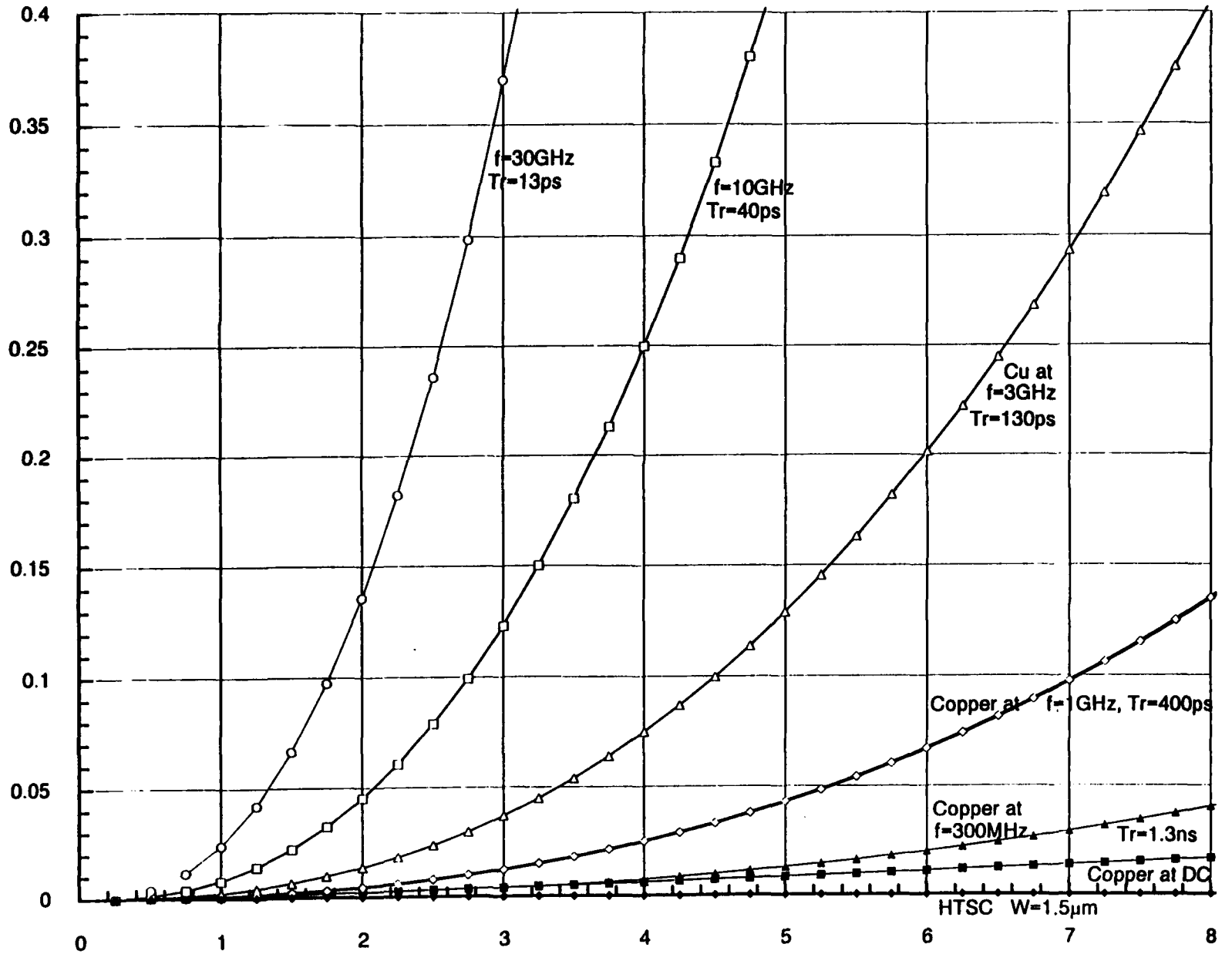
Rmax=25Ω 10K-Gate (370 I/O) Flip-Chip Max-Density MCM Comparison of HTSC to 77°K Copper Interconnects vs. Frequency



Horizontal is Edge Size of MCM in inches, Vertical is Number of Signal Layers Required to Complete Inter-Chip Wiring

Figure 10

Tmat for Rmax=25Ω 10K-Gate (370 I/O) Flip-Chip Max-Density MCM Comparison of HTSC to 77°K Copper vs. Frequency



Horizontal is Edge Size of MCM in inches, Vertical is Thickness of Wiring Mat in inches for Zo=50Ω, Er=3.9 Dielectric

Figure 11

risetime), $L_{eq} = 5.07$ cm (or $X_M = 1$ inch MCM size). Note in both Figures 8 and 10 that the 300MHz ac curves of S vs. X_M depart from the dc curves above $X_M = 3.3$", and the 1GHz ac curves above about 1" as calculated from Eq. 9. In terms of signal layer requirements, the $R_{max} = 25\Omega$, 300°K Cu case plotted in Fig. 8 is similar to the $R_{max} = 10\Omega$, 77°K Cu case plotted in Fig. 6, and need not be discussed further here. The most favorable case for copper is, of course, the 77°K cooled copper case with the relaxed $R_{max} = 25\Omega$ (partially self-terminated lines) ohmic line resistance specification. As seen in Table 4 and Figure 10, an $X_M = 6$ inch maximal-density MCM carrying 576 10K-gate flip-chip-mounted 370-I/O VLSI die having Tr = 0.4ns signal risetimes (reasonable for cooled CMOS) would require over 32 layers of 77°K copper interconnects, or 49 total metal layers (including power/ground planes) in a wiring mat about $t_{mat} = 1.7$mm (0.067") thick to complete the 1.94 miles of inter-chip wiring on the MCM. By the mid to late 90's, cooled short-channel CMOS risetimes will likely be several times faster than this, corresponding to signal frequencies in the 3GHz range. As seen in Figs. 10 and 11, the 6" MCM at this speed would require 55 cooled copper signal layers of $W = 41\mu$m width to achieve the $R_{max} = 25\Omega$, or about 84 total metal layers in a $t_{mat} = 5.1$mm (0.20") thick wiring mat. Hence, even in this most favorable case for copper, the number of interconnect layers required would appear to be impractically large from a manufacturability/yield standpoint. Further, using such an $R_{max} = 25\Omega$ self-terminated line approach would, for good signal integrity characteristics, probably require a number of different driver types, each having different source resistance characteristics, thereby complicating the design task.

As is pointed out in Ref.1, Section 3.1, plain $R_{max} = Z_o$, open circuit load/source terminated interconnections can tolerate somewhat over $R_{max} = 10\Omega$ line resistances without major degradation of the substantial CMOS noise margins. From that standpoint, ohmic line resistances of $R_{max} = 25\Omega$ represent, with true open-circuit loads, only a very modest degradation of pulse propagation characteristics. However, when the rather significant input capacitances which load the lines is considered, pulse edges with source termination are degraded relative to load termination, and that is made even worse when higher resistance, self-terminated lines are used. Consider, for example, a 10pF load capacitance on

an R_L = 50 Ω terminated line, which will have a 550 ps rise time, but with a Z_o = 50Ω source-terminated line, the rise time is 1.1 ns. Hence, while source termination is convenient and low power, it has high speed performance limitations relative to load termination, which are only further aggravated as self-termination is approached.

A final potential method of reducing the number of copper layers required to wire large maximal density MCMs is to relieve the constraint that all lines have the same width. In IC design, it is common to use narrower (higher Ω /cm) lines for the (numerous) shorter lines, and the wider line widths only for the longer lines. Unfortunately, in a MCM, simply increasing the line width alone doesn't help at all, since it correspondingly reduces the line impedance, Z_o, which makes the line proportionately more sensitive to R_{max}. However, if the dielectric layer thickness is increased in the same proportion, the line impedance will be preserved and the desired relative line ohmic resistance improved. Hence, it would be possible in an MCM to create two or more classes of signal interconnects, with wide copper traces and thick dielectrics for long lines and (higher density) narrower traces with thinner dielectrics for short lines. While this would require some substantial innovations in order for the CAD tools (particularly MCM routers) to support such an interconnect hierarchy (and routing software is already a serious problem for very complex boards), it is certainly theoretically possible to implement such an approach. While its practicability might be in question, the fact that there are so many short wires on a MCM makes it of interest. As opposed to the maximum signal line length of L_{max} = 12" on a 6" MCM, as seen in Tables 1 - 4, the average wire length, R_{bar}, for the same case is only (R_{bar} = 4.608 chip pitches of X_p = 0.635 cm for N_R = 24) $\bar{L}$ = 2.93 cm (1.15"). Hence, from Eq. 5 for 10^9 Hz and R_{max} = 10Ω, a 77°K copper line width of W = 5.74μm would be adequate for half of the interconnect wires. Since from Table 2, S = 80 layers of W = 59μm cooled copper interconnects would be needed for all of the wiring, from Eq. 2, using W = 5.74μm for short lines would mean that half of the MCM wires could be disposed of in 4 layers of signal interconnects, which would make a substantial reduction in the total number of signal layers required. Unfortunately, it is not quite that simple. The longest (L_{max} = 12") class of 77°K copper wires must be over 10 times wider (59.4μm/5.74μm) and the dielectric layers

10 times thicker than for short lines. In general, vias and other layout features of a size adequate for thick dielectric layers and large trace sizes are not very compatible with interconnects an order of magnitude smaller in feature sizes. (Eg., via contact diameters are often 2 or more times the linewidth, so for the long lines they might be 120μm to 150μm or more in diameter, which is enormous in comparison to the W=5.74μm width of the short lines discussed above.) Hence, real design rule limitations will play a major role in how effective such a hierarchial dielectric thickness/variable line width approach would be in reducing the number of 77°K copper signal interconnect layers required to wire large maximal density MCMs. A wild guess might be a 2x reduction over the constant width case, but it certainly depends on the details of the layout design rules for the MCM technology.

In summary, several new normal metal interconnect MCM technology extensions have been considered which, if developed and adopted, could potentially reduce significantly the number of copper interconnect layers required to wire large, maximal density MCMs. If all of these (cooling to 77°K, using high resistance [self-terminated] interconnect lines, and routing in a hierarchy of dielectric layer thicknesses and line widths according to signal line length) were used at the same time, and if the rise times of the logic signal pulses were fairly slow, then it might even be possible to reduce the number of copper interconnect planes to something which might be manufacturable (given the existence of very effective in-process inspection and repair capabilities, and, of course, assuming that the very large stress levels that build up in organic dielectric MCM systems at cryogenic temperatures don't give insurmountable reliability problems). However, if this can all be done in a simple, two signal layer HTSC MCM, which will work with today's CAD tools (routers, etc.), which will work with any kind of signal interconnect termination scheme (eg., source or load terminated), and which will work with even the fastest of today's integrated circuit technologies, and indeed with the fastest expected in the foreseeable future, and do all of this without the performance and design compromises discussed above, and further yet be potentially cheaper, in the long term why would anyone want to consider anything short of the HTSC MCM technology? The issue is not whether HTSC MCMs are worth doing, it is whether we can in fact master the technology to build them.

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Section 2.0

Commercialization of High Temperature Superconducting Technology

2.1 Background

Discussions with Tony Vacca, Frank Patton, and colleagues in the industry and government labs have convinced me that the program in HTSC MCM should really be viewed from a much broader perspective. HTSC MCM is in fact part of the larger field of cryoelectronics. Richard Eden had clearly demonstrated that the combination of HTSC MCM and cooled CMOS could eventually yield an order of magnitude increase in performance over a corresponding room temperature CMOS system. With the cost of building a foundry dramatically increasing (where now it would exceed $1B) and with the cost of cryogenic decreasing, maybe the time has come to start looking at cryoelectronics as a real business. As has been stressed before, the survivability of HTSC companies is at risk unless a sizeable market is found that these small companies can address. Since these companies need to cool the electronics anyway, it may make sense that while they are developing the HTSC technology, they can start now looking into the possibility of building products which are non-superconductive. Non-superconducting cooled CMOS based system may be a viable business. These small companies having the cryoelectronics capabilities (cryogenics, testing, packaging, cycling, etc.) could provide new performances using current CMOS technology but optimized to operate at liquid nitrogen could make available to these companies a significant market niche and render these HTSC companies as part of the semiconductor community. In January we held a work shop in San Jose at N-Chip on this subject. There seems to be a consensus of this thinking. We have spoken to E-Systems and Cray about using the E-L machine as a test bed and to N-Chip about testing the Ross RISC processor at LN temperature. Discussions with semiconductor houses and other companies producing CMOS systems will continue to evaluate the possibility of converting room temperature systems into cooled systems. Commercial and military applications will be considered.

3.2 Q1 1992 Quarterly Report

Section 1.0

MCM Line Resistance Requirements as Determined from Lossy Line Transient Response Characteristics

1.1. Background

As discussed in several of the quarterly reports and in the final report to the first portion of this effort, the primary interest in HTSC interconnects in MCMs stems from the difficulty of obtaining adequately low signal line ohmic resistances using fineline metal interconnects. In the initial analysis of the required number of signal layers versus MCM size for a maximal density, Rent's rule I/O count limited MCM, a maximum dc end-to-end line resistance of 10 Ω was assumed to give adequate digital pulse propagation characteristics (dynamic noise margins) for either source-terminated, open-load (CMOS-type) or for load-terminated (ECL - type) signal interconnect schemes for assuming transmission line characteristic impedances of the order of Z_0 = 50 Ω. It was subsequently noted that because of the substantially faster clock rates and signal edge rates possible with advanced integrated circuit technologies, such as short channel CMOS, particularly when operated at cryogenic temperatures, the relevant high frequency ac skin depth, δ can be considerably smaller than the signal conductor dimensions, making the ac resistance much larger than the dc resistance. In the final report and the last quarterly report (Q4 1991), the plots of the required number of signal layers for copper interconnects were made for dc and for ac frequencies of 300MHz, 1GHz, 3GHz, 10GHz and 30GHz, for total worst case dc and ac resistances less than either 10Ω or 25Ω for either 300°K copper or 77°K copper interconnects. A "rule of thumb" f = $0.4/t_r$ relationship between digital signal risetime and equivalent ac signal frequency was noted for each of the frequency curves in the four figures.

While this simple association of risetime, signal frequency and a maximum allowable ac resistance specification for acceptable signal quality is a convenient extension of the simple maximum allowable dc trace resistance concept, it is not as rigorous or quantitative as the dc specification. The problem is that while a pulse train at some clock frequency f_c with a risetime, t_r, certainly has strong frequency components up to at least $3f_c$ or $5f_c$, or up to frequencies of the order of $f = 0.4/t_r$, these higher frequency components do not appear with 100% of the signal amplitude, and hence a given level of attenuation of these components is not necessarily as serious as an attenuation of the fundamental, or dc component, by the same amount. Hence, a specification that the ac skin effect line resistance at the third or fifth harmonic of f_c, or at $f = 0.4/t_r$, must be, for example, $\leq 10\Omega$ may be unecessarily severe.

The only way to quantatively resolve the issue of what conductor size is required for a given length of interconnect in order to achieve adequate dynamic noise margin characteristics under specified signal risetime, etc., conditions is to know accurately the time-domain (as opposed to frequency domain) response of the lossy line. For the case of linear driver and load characteristics (ie., driver and load impedances which are linear in signal amplitude and not time dependent, but which may be frequency dependent, and impulse response for the lossy line path may be derived, and the output waveform obtained as the convolution of the impulse response with the input waveform. In the spirit of the rest of the analysis work on the HTSC MCM advantages/requirements, we would like to come up with simple analytic expressions or standard numerical calculation methods that anyone can verify, extend or apply to other cases of interest "in the comfort of their own home or office", so to speak. This is as opposed to simply buying the appropriate CAE tools for a suitable engineering workstation and running these to get the transient lossy line outputs for specific cases of interest. (Quad Design, of course, has only encouragement for those with the budget resources and inclination to take the easy way out and use their XTK [Crosstalk Tool Kit] suite of CAE software tools including the XFX [Crosstalk Field Extractor] and XNS [Crosstalk Network Simulation] tools to take this approach.)

This bit of "tongue in cheek" aside, it should be noted that the purpose of this effort is to derive insight which guides the design process by fitting a limited number of accurately numerically treated specific cases and/or analytic expressions. These case may be idealized and simplified as required to illuminate the essential elements of the design problem. This is quite different from the (*far* more difficult) problem for which the Quad Design tools were developed. These tools were designed to execute very computationally intensive design evaluation tasks within an acceptably short time on reasonably-priced workstations. For example, they can handle multiple conductors of arbitrary geometry, multiple segments of transmission line of different geometry in complex paths, and (the very difficult case of) real nonlinear IC output driver and input receiver lossy transmission line sources and loads. They are designed to execute these analysis in an "automatic" fashion from board or MCM design databases on large numbers of real, complex interconnect nets and furnish the analysis results (eg. time domain response data, delay times, rise/fall times, undershoot/ringing characteristics, etc.) for use in higher levels of design evaluation (eg., timing verification or logic simulation). This requires an *extremely* efficient implementation of computational approaches in order to give engineering quality results in an acceptable time without requiring a CRAY C-90 supercomputer to run the job. This necessitates, of course, both some cleverness in obtaining very high calculational efficiency, and some engineering approximations in favor of faster simulation time where the sacrifices in accuracy are not generally significant for real designs. However, for an analytical fitting of the type we are interested in here, focus may be extended into such "extreme" regions in which the engineering tools may not furnish the desired levels of precision. For this reason, a much slower, but "proof quality" result for simple single lines with linear source and load is better for our purposes.

1.2. Simple Approaches to Lossy Line Transient Response

1.2.1. Coaxial Line Example

Figure 1 illustrates the methods used for calculating the resistive line loss contribution to transmission line response for the simple case of a coaxial line. For the purposes of our analysis, we will assume the dielectric within the line is ideal, that is, lossless and non-dispersive (a frequency-independent dielectric constant, ε_r), with a value of $\varepsilon_r = 3.90$ taken for the numerical example (eg., SiO_2 or typical polyimide). If the coaxial center conductor (signal line) and outer shield (ground) were ideal, that is, had zero resistivity, $\rho = 0$, then the line would have a distributed external inductance (inductance per meter) of

$$L_{ext} = \frac{\mu_o}{2\pi} \ln\left(\frac{R_b}{R_a}\right) \qquad \text{for } \delta = 0 \qquad (1)$$

valid where the skin depth, δ, given by (Ref. 1)

$$\delta = \frac{1}{\sqrt{\omega \mu_o / 2\rho}} \qquad (2)$$

is very small compared to the dimensions of the conductor (R_a and $R_o - R_b$ in Fig. 1). It is assumed here that the dielectric and conductor materials are non-magnetic, that is $\mu = \mu_o = 4\pi \times 10^{-7}$ henrys/meter. For this case, the capacitance per meter of the coaxial line is given by

$$C = \frac{2\pi \varepsilon_o \varepsilon_r}{\ln\left(R_b/R_a\right)} \qquad (3)$$

where ε_o = 8.85418782 x 10^{-12} farads/meter, and the high frequency ($\delta \approx 0$) characteristic impedance of the coaxial line with center conductor radius of R_a and inner shield radius of R_b is given by

$$Z_o \equiv \sqrt{L/C} = \eta \sqrt{\mu_o/\varepsilon_o} \quad \frac{1}{2\pi\sqrt{\varepsilon_r}} \ln\left(\frac{R_b}{R_a}\right) \qquad (4)$$

where $\eta = \sqrt{\mu_o/\varepsilon_o}$ = 376.7303134 ohms is the impedance of free space. For the case treated numerically here, with R_b = 6.59200577 x 10^{-5} meters gives, with ε_r = 3.90, Z_o = 50Ω.

1.2.2. R_{dc} - Only (Low Frequency) Lossy Coax Response

At the other extreme to the $\delta \approx 0$ case discussed above is the low frequency "dc" case where the skin effect penetration depth, δ, is large in comparison to the conductor dimensions ($\delta > R_a$ and $\delta > R_o - R_b$). Here the signal current density is not confined just to the thin surface regions of the conductors (darkly shaded in Fig. 1'), but rather the current flows uniformly over the conductor area. In this case there is additional line inductance, L_{int}, due to the presence of magnetic fields within the conductors. For the round center conductor in the coax this "internal" inductance is given by

$$L_{int}\,(dc) = \frac{\mu_o}{8\pi} \qquad \text{for } \delta >> Ra \qquad (5)$$

Also, the effective radius of the outer conductor used to calculate the external inductance in Eq. 1 should be about $R_b' \approx \left(R_b + R_o\right)/2$. The total low frequency inductance is just the sum of L_{ext} from Eq. 1 and L_{int} from Eq. 5. For the line dimensions cited above, with R_o = 8.128 × 10−5 meters outer shield radius (Fig. 1), the coaxial line inductance would increase from L_{ext} = 329.368 nH/meter at high frequency ($\delta \approx 0$) to L_{dc} = 401.409 nH/meter (50nH/meter increase from

the center conductor and the remainder due to the increase in effective shield radius, R_b') at low frequency. This would increase the line impedance from $Z_o = 50\Omega$ at high frequency to 55.198Ω at low frequency (a 10.4% increase). The velocity of propagation, given for the lossless case by

$$v_p = 1/\sqrt{LC} = c/\sqrt{\varepsilon_r} \qquad (6)$$

(where $c = 2.99792458 \times 10^8$ meters/second is the speed of light) will also be altered by the change in inductance, from $1/v_p = 6.587363$ns/meter (167.319ps/inch) at high frequency to about $1/v_p = 7.272$ns/m (184.7ps/inch) nominally at low frequency if Eq. 6 were still valid (with $L = L_{ext} + L_{int}$) for this $\delta >> R_a$ and $S >> R_o - R_b$ case. However, in the presence of substantial line loss the pulse propagation gives rise to distortion and attenuation of input pulses which make it more difficult, in general, to define a velocity of pulse propagation for the line. The purpose of the lossy line response analysis is to calculate the actual transient output waveform, which includes both velocity and dispersive attenuation distortion effects on pulse waveforms.

As was discussed in the first quarterly report on this contract (reproduced as Appendix 1 of the final report of 10/91), the dc line resistance is of obvious importance for the case of load-terminated interconnect lines due to gross loss of dc noise margin because of the ohmic line resistance/load termination resistance voltage divider action. If the dc line resistance exceeds 10 or 15 Ω, the ECL noise margins are seriously compromised (unless full differential signal transmission is used). As was discussed in that report, while there is obviously no problem with ohmic line resistance at dc if the CMOS like source-terminated/open load configuration is used, the tolerance for line resistance for ac or fast transient signals is only a little better than for the load-terminated case.

Because of skin effect, the ac line resistance, as illustrated in Fig. 1, is generally much higher than at dc. At first glance, this could lead one to think that, for fast risetime signals (which carry very high frequency components), the dc line

resistance, R_{dc}, would not be important. However, when it is noted that for a 1 foot length (30.48 cm) of coax, the current pulse to a step input on the t_{pd} = 2ns length of line is $\Delta t = 2t_{pd}$ = 4ns wide, we see that even if the input pulse risetime is 40ps, representing frequency components near 10GHz (where the skin effect depth in room temperature copper is only $\delta = 0.656\mu m$), the full envelope of the 4ns current pulse requires a low frequency bandpass, for negligible (eg. 2.5%) droop, of 1MHz (assuming single pole rolloff), at which frequency δ = 65.6μm (2.58 mils; larger that the conductor dimensions in the coax example).

The effect of R_{dc} (only) on the transient response of the 1mil diameter center conductor Z_o = 50Ω coax was evaluated for lengths of 6", 12", 18" and 24" in the 50Ω source resistance open circuit load configuration using PSpice. For purposes of calculation the internal inductance effects were ignored (Z_o kept at 50Ω and v_p unchanged). The transmission line was broken into 10ps long segments (eg. 200 segments to model the 12" line, 400 for the 24", etc.) with a R_{dc} = 0.0546034Ω resistance placed in series with each Z0 = 50, TD = 10P transmission line segment. PSpice transient simulations with a 10ps risetime input step were carried out using a 5ps or less iteration step size. Run times were slow (≈ 100 seconds/ns for the 12" line on a MacIIfx), as expected for SPICE, in comparison to the streamlined Quad Design tools which also include skin effect and are therefore more accurate as well. These PSpice R_{dc} (only) lossy line response simulations are plotted, along with other simulations, in Figs. 7 through 15. Since they ignore skin effect, the R_{dc} curve is generally the highest curve in each of the figures. Fig. 12, for a 24" (60.96cm) line length of the 1mil copper coax, illustrates the R_{dc} (only) response. The initial output step amplitude after the t_{pd} = 4ns line delay is 80.38% of the input voltage step (it would be 100% if the line were lossless, of course). This initial step amplitude is given from the total dc ohmic line resistance, R_{dc}, (eg. R_{dc} = 21.84136Ω for the 24" example of Figs. 12 and 13) by

$$V_{out}\left(t_{pd}\right) = V_{in} e^{-\frac{R_{dc}}{2Z_o}} \qquad \text{for } R_{dc} \text{ (only)} \qquad (7)$$

where V_{in} is the input step amplitude and t_{pd} is the propagation delay time of the line (4ns in Fig. 12). As seen in Fig. 12, the step response for R_{dc} (only) increases approximately linearly (it is probably exponential-like) over the next 2 t_{pd} to a second break point at $t = t_{pd}$ (from the initial input step) at which the output amplitude is given, at least approximately, by

$$V_{out}(3t_{pd}) = V_{in} e^{-0.12\left(\frac{R_{dc}}{Z_o}\right)^2 \left(\frac{V_{out}(t_{pd})}{V_{in}}\right)} \qquad \text{for } R_{dc} \text{ (only)} \qquad (8)$$

where the quantity $V_{out}(t_{pd})/V_{in}$ in the exponential expression is found from Eq. 7. The numerical value of 0.12 in Eq.8 was determined by fitting the data for the four line lengths analyzed, and gives an accuracy for $V_{out}(3t_{pd})$ of $\pm 0.005\%$ for the cases treated. Beyond this $t = 3\ t_{pd}$ break point (at 12ns in Fig. 12), V_{out} extrapolates more or less linearly to essentially V_{in} at $t = 5\ t_{pd}$ (20ns in Fig. 12).

Eqs. 7 and 8 for the R_{dc} (only) response break points apply most accurately to the cases of most interest; that is, where R_{dc} us substantially smaller than Z_o (so the line transient response is favorable). Just for interest, a high resistance case corresponding to 12" of about 0.3 mil coax, with a total $R_{dc} = 100.0\Omega$ or $R_{dc}/Z_o = 2$ for a 12" line was analyzed and found to fit Eqs. 7 and 8 fairly accurately (0.25% for Eq.7 and 1.9% error for Eq. 8) even though it is in the highly lossy (erfc-like step response) region (very slow risetime beyond the initial step). As will be discussed later, the combined skin effect plus dc ohmic resistance lossy line response can be at least approximated by a convolution of the skin effect response (with $R_{dc} = 0$) with this R_{dc} (only) response. While the R_{dc} (only) curves in Figs. 7-15 were obtained using PSpice simulation, simple linear interpolation between the breakpoint values given above (at $t = t_{pd}$ in Eq. 7, $t = 3t_{pd}$ in Eq. 8 and $V_{out} \approx V_{in}$ at $t = 5t_{pd}$) should be quite adequate to define the R_{dc} (only) response without PSpice.

1.2.3. Skin Effect Only (R_{dc} = 0) Lossy Coax Response

In general, due to the non-uniformity of current density on the surface of conductors in transmission line configurations, 2-d solver numerical methods are required to get accurate values for the frequency-dependent ac (skin-effect) resistances of lines (ie. to determine the current "filling factor"). For the particular case of a coaxial line, illustrated in Fig. 1, the magnetic field strengths are uniform over the surfaces of the center conductor and the inside of the outer shield, and the field strengths are easily calculated (falling as the inverse of the radial distance). Hence, as shown in Fig. 1, the frequency-dependent ac (skin-effect) resistance can be easily calculated for this case, assuming the frequency to be high enough so that the penetration depth, δ in Eq. 2, is much smaller than the conductor dimensions (fully developed skin effect condition). The frequency-dependent skin effect resistance, R_{ac} in Fig. 1, is given by

$$R_{ac} = \frac{\rho}{2\pi\delta}\left(\frac{1}{R_a} + \frac{1}{R_b}\right) \quad \text{for } \delta << R_a, (R_o - R_b) \qquad (9)$$

(for R_{ac} in Ω/meter), and the internal inductance, L_{int}, due to the skin effect is given for the angular frequency, ω, by [Ref. 1]

$$L_{int} = R_{ac}/\omega \qquad \text{for } \delta < R_a, (R_o - R_b) \qquad (10)$$

(for L_{int} in henrys/meter, but the inverse Fourier transform necessary to convert the frequency domain results to a time domain step response is known in closed form for this fully developed skin effect case. The distributed inductance, L_{ext}, of a lossless line gives rise to the distributed reactance of the line

$$Z_{ser} = j\omega L_{ext} \qquad \text{(lossless line)} \qquad (11)$$

For the lossy case, this becomes

$$Z_{ser} = j\omega L_{ext} + j\omega L_{int} + R_{ac}$$
$$Z_{ser} = j\omega L_{ext} + R_s \sqrt{j\omega} \qquad \text{(full skin effect)} \qquad (12)$$

where the $R_s \sqrt{j\omega}$ term includes both the real part, R_{ac} from Eq. 9 and the inductive part, L_{int}, from Eq. 10. Note that, from the 45° angle of this skin effect term,

$$R_s = \frac{\sqrt{2}\, R_{ac}}{\sqrt{\omega}} \qquad (13)$$

This definition of R_s is the same as that used by Rubin in Ref. 3. Gardiol (Ref.2) does an analysis for the case of an air coax line (instead of filled with a dielectric constant, ε_r), and unfortunately uses the symbol Z_o in place of η (see Eq. 4). Converting his notation to the notation used here and in Ref. 3, Gardiol's distance parameter, z, equals $x\sqrt{\varepsilon_r}$, where x is the physical distance down the line in meters, and Gardiol's constant "k" (as in the term $-kz\sqrt{j\omega}$ in his Eq. 10.25) is equal to $R_s / (2 Z_o \sqrt{\varepsilon_r})$, where Z_o is the line impedance (eg. 50Ω). Gardiol gives the step response for this fully developed skin effect case at position, z, and time, t, as

$$u(z,t) = \text{erfc}\left(\frac{kz}{2\sqrt{(t - z/c)}}\right) \qquad \text{for } t \geq z/c \qquad (14)$$

where erfc is the complementary error function, plotted in Fig. 2 for convenient reference, and c is the speed of light. Converting this step response expression to our notation,

$$u(x,t) = \text{erfc}\left(\frac{R_s x}{4 Z_o \sqrt{t - x/c_{eff}}}\right) \qquad \text{for } t \geq x/c_{eff} \qquad (15)$$

where x is the physical distance from the source end of the line in meters and $c_{eff} = c/\sqrt{\varepsilon_r}$ is the speed of light in the dielectric. R_s is given for the coax case by Eqs. 13 and 9 as

$$R_s = \frac{1}{2\pi}\sqrt{\mu_o \rho}\left(\frac{1}{R_a}+\frac{1}{R_b}\right) \tag{16}$$

for $\delta << R_a$ abd $\delta << R_o - R_b$; Eq. 15 may also be written using a time normalizing parameter, t_{sel}, as

$$u(x,t) = \text{erfc}\left(\frac{1}{\sqrt{t'/t_{sel}}}\right) \qquad \text{for } t' > 0 \tag{17}$$

where $t' = t - x/c_{eff}$ is the time measured relative to the nominal pulse arrival time, and t_{sel} must be given by (from Eq. 15)

$$t_{sel} = \left[\frac{xR_s}{4Z_o}\right]^2 \tag{18}$$

The complementary error function, plotted in Fig. 2 for reference, may be approximated for small values of the argument as

$$\text{erfc}(x) \approx 1 - 1.12837878x \qquad \text{for } x << 1 \tag{19}$$

Eq. 19 is 0.1% accurate to x = 0.054, 0.5% to x = 0.123, 1% to x = 0.174, 2% to x = 0.246, 5% to x = 0.396 and 10% to x = 0.574.

Since most of the electrical response issues concern the "tail" of the response function where erfc(x) is nearing unity (x is small), Eq. 19 is a very useful approximating function for cases of interest. (Remember that in Eq. 17 the square root of time is in the denominator, so large time is small x.) In this "tail" region of Fig. 2, the complimentary error function may be approximated by

$$\text{erfc}(x) \approx 0.48235\, e^{-1.23946361x^{1.9}} \quad \text{for } 1 < x < 5 \qquad (20)$$

This approximation is good to ±1.25% for $1.596 \leq x \leq 4.332$, ± 5% for $1.30 \leq x \leq 4.704$, and ± 10% for $1.05 \leq x \leq 5.02$. Since the lossy line step function expression in Eqs. 14, 15 and 17 involve a square root, it would be more convenient if the exponent of x in Eq.

20 were 2, instead of the more accurate 1.9. A reasonably good fit for this tail region of the erfc curve is given by

$$\text{erfc}(x) \approx 0.419\, e^{-1.10x^2} \qquad \text{for } 1 \leq x \leq 3.2 \qquad (21)$$

This expression is accurate to ± 10% for $1.035 \leq x \leq 3.174$, or +10%, -20% for $0.7292 \leq x \leq 3.478$. Eq. 21 is very useful for the initial rise portion of the fully developed skin effect response function . For example, using the approximation of Eq. 21, the voltage response of Eq. 17 becomes simply

$$u(x, t) \approx 0.419\, e^{-1.10\ (t_{sel}/t')} \qquad \text{for } 0 < t' \ t_{sel} \qquad (22)$$

where $t' = t - t_{pd} = t - x\sqrt{\varepsilon_r}/c$ and t_{sel} is given by Eq. 18. Eq. 22 is very useful for picking off the 10% or 20% response points for a 10% - 90% or 20% - 80% risetime calculation, for example. The other end of the curve, where the 90% or 80% points would be picked off can be approximated by using Eq. 19 in Eq. 17, or

$$u(x,t) \approx 1 - 1.12838\ \sqrt{t_{sel}/t'} \qquad \text{for } t' > 33\, t_{sel} \qquad (23)$$

which is 1% accurate for $t' > 33\, t_{sel}$ (near the 80% point), and 0.25% accurate near the 90% point ($t' > 126\ t_{sel}$). For convenience in other regions where these approximations are not very accurate, the erfc $(1/\sqrt{t'/t_{sel}})$ function is plotted versus

t'/t_{sel} for the ranges of $0 \le t'/t_{sel} \le 35$ in Fig. 3, $0 \le t'/t_{sel} \le 150$ in Fig 4, $0 \le t'/t_{sel} \le 750$ in Fig. 5.

Standard inexpensive engineering/scientific mathematical packages such as Bimillenium Corporation's "HiQ" or Wolfram Research's "Mathematica" for Macintosh computers have efficient built-in erfc (x) functions, as well as solvers that can provide inverse values (ie. extract crossing times). (The material for Figs. 2-15 here were calculated using "HiQ", except for the R_{dc} [only] curves [from PSpice] and Quad XNS simulations.)

1.2.4. Comparison of Idealized Coax Cases to XFX and XNS Results

Getting all of the stray $\sqrt{2}$ (or $\sqrt{\varepsilon_r}$ or larger) factors in Fig. 1 or the foregoing equations (particularly Eqs. 13 - 18) exactly right is fairly demanding, so it is very valuable to check these expressions again' standard engineering tools for correctness. Since the coax case shown in Fig. 1 and applicable to Eqs. 1, 3, 4, 5, 9 and 16 (the other equations are general) is the only one not requiring 2-d solver numerical techniques to get R_{ac} or R_s values accurately (Eqs. 9 and 16), this case was used. The first step was to extract the R_{dc} and R_s (ac) lossy line parameters (along with characteristic impedance etc.) using the XFX part of the Quad Design XTK tool kit. Note that a coax line is a very difficult case to solve with high accuracy on a rectangular conductor grid solver (which is optimal for "real" MCM or circuit board interconnects like stripline or microstrip). The materials values taken were ρ = $1.70 \times 10^{-8}\Omega$-m for 300°K copper and ε_r = 3.90 for the dielectric, with the Z_o = 50Ω line geometry scaled from a 1 mil diameter center conductor (Ra = 1.27×10^{-5} m, R_b = 6.592×10^{-5} m and R_o = 8.128×10^{-5} m, as defined in Fig. 1). Overall grid sizes for the XFX calculation of 200 x 200, 400 x 400, 600 x 600 and 800 x 800 points were evaluated for mesh sensitivity. The R_{dc} and Z_o results were quite accurate from XFX; eg. Z_o = 49.98Ω even for the coarsest (200 x 200) mesh case. R_{dc} values for the 4 mesh sizes were 0.35829Ω/cm, 0.35836Ω/cm, 0.35847Ω/cm, and 0.35851Ω/cm respectively, versus a value of 0.35943245Ω/cm calculated analytically

(Fig. 1), corresponding to absolute errors from 0.26% for the 800 x 800 mesh up to 0.30% for the 200 x 200 mesh. The numerical problem is a lot tougher for the ac skin effect resistance, reported as R_{sij} by the XFX program, because it is "texture" sensitive and the texture of a small circle is poorly represented by a rectangular grid. the R_{sij} values obtained varied from 0.44001 for the 200 x 200 grid, 0.44442 for 400 x 400, 0.49029 for 600 x 600 and 0.55318 for the 800 x 800 grid, with the units indicated as $\Omega\sqrt{ns}/cm$. These values were (finally) compared to a nominal analytic value for R_{sij} = 0.48847978 for this quantity, so that the four numerical results represent errors of -10%, -9%, +0.37% and +13.25% respectively (not unreasonable, considering the highly unfavorable geometry for the numerical approach).

A more difficult problem was understanding just what XFX was reporting for this $R_s$ij quantity and how it relates to R_s or R_{ac} (Eqs. 16, 13 and 9). For this example, we have, from Eq. 16, $R_s = 2.184548 \times 10^{-3}\ \Omega\sqrt{s}/meter$. Unfortunately, despite the similarity of notation to R_s in Ref. 3 or in Fig. 1 or Eqs. 13 or 16 here, the XFX definition of R_{sij} is given by

$$\text{(XFX)} \qquad R_{sij} = \frac{R_{ac}}{\sqrt{\omega \times 10^{-9}}} = \frac{R_s}{\sqrt{2 \times 10^{-9}}} \qquad (24)$$

Hence, the Eq. 16 value of $R_s = 2.184548 \times 10^{-3}\ \Omega\sqrt{ns/m}$ divided by $\sqrt{2 \times 10^{-9}}$ becomes $R_{sij} = 48.8479783\ \Omega\sqrt{ns/m}$ or the $R_s$ij $= 0.4884798\ \Omega\sqrt{ns/cm}$ value cited above (which is in the center of the range of the XFX calculated values). Because the XNS simulator accepts as input the line parameters extracted by XFX, and we wanted to use analytically accurate values for R_s in the comparisons between the transient waveform calculations here and the XNS waveform simulations, the analytic R_{sij} value was used as input to XNS for all simulations of the 1 mil center conductor copper coax line (Figs. 6-15).

As a check of the fully developed skin effect (only; $R_{dc} = 0$) step response expressions (eg., Eqs. 14-18), XNS was run with $R_{sij} = 0.48848$ and $R_{dc} = 0$ (obviously non-physical unless the center conductor of the coax had a room

temperature superconducting core) for a 12" (x = 0.3048m) line length of Z_o = 50Ω coax with a 50Ω source resistance and open load, using a 1ps risetime input and a 1ps step size. From Eq. 18, t_{sel} = 11.0839ps for this line length, and the step response expression in Eq. 17 was evaluated with a 1ps step size for comparison to the XNS simulation. The results are compared in Fig. 6. Aside from an apparent artifact in XNS that the first 8 time points (past t_{pd} = 2ns, of course) were printed as zero values (they all had values under 10% of the input step and were somehow ignored in the output), the erfc ($1/\sqrt{t'/t_{sel}}$) and XNS values compared very accurately to 20 or 30 ps, with XNS falling below the analytical expression by 2.7% to 2.9% at larger times. The reason for this small difference has not been identified, but it could involve either computational shortcuts in XNS or the fact that XNS treats the full (incident and backscattered) propagating wave conditions, while Eq. 17 assumes only a forward propagating waveform. In any event, the agreement in Fig. 6 is quite good between XNS and the analytic functional form of Eq. 17.

1.2.5. Lossy Line Transient Response Calculations with Both R_{dc} and Skin Effect - Practical Approach

As was discussed in section 1.2.2, because even fast risetime step signal require low frequency components to accurately represent them (frequencies for which the skin effect depths will typically exceed the conductor dimensions), both the dc (R_{dc}) and the skin effect (R_s) losses must be included to obtain accurate results for real lossy lines. Unfortunately, the inverse Fourier transform to convert lossy line frequency response to time domain transient response, which is known in closed analytic form for the fully developed skin effect case (Eqs. 14-18), is not known in closed analytic form for the mixed R_{dc} + skin effect case. In fact, in general even the frequency domain response is not well known in the "crossover" region between low frequencies (where R_{dc} dominates) and high frequencies (where R_s dominates), (ie., where the skin effect depth [δ in Eq. 2] is comparable to the conductor dimensions). The frequency dependence is known analytically for the round wire center conductor in coax, but the Bessel function solutions [Ref. 1 or Ref. 2] are fairly complicated. In Section 2.4 of the October 1991 Final Report for this contract,

approximate analytic expression for the frequency dependence for microstrip and stripline conductor geometries were developed which would be very helpful for use with numerical methods for obtaining the inverse Fourier transform (IFT) to get the time domain response. Analytic closed form expression for the IFT step response are unlikely, however.

In the real world of engineering difficult theoretical or computational problems must somehow be dealt with in a "good enough" practical way that gives adequate accuracy for the intended engineering purpose of the tools. The approach used in the Quad XNS tool to simultaneously include both skin effect and R_{dc} line loss contributions is alluded to in Ref. 3. Figs. 7-9 compare the results of the XNS calculation for the 12" open coax example described previously (done with a 10ps input risetime and 10ps step size) with the fully developed skin effect expression from Eq. 17 [erfc $(1/\sqrt{t'/t_{sel}})$], and with the R_{dc} (only) results from the PSpice simulations discussed in Section 1.2.2. As would be expected, both the R_{dc} (only) and skin effect (only) curves are too optimistic, since each omits an important part of the loss (see Fig. 9, for example).

The real line response would involve some type of convolution between the R_{dc} (only) and erfc $(1/\sqrt{t'/t_{sel}})$ skin effect (only) curves in Fig. 9. Since the R_{dc} curve is fairly flat, a good first guess at the combined response is just to do a point by point multiplication of the R_{dc} (only) curve with the erfc $(1/\sqrt{t'/t_{sel}})$ curve (Eq. 17). This combined curve, noted as R_{dc}*erfc in Figs 7-15, falls in fact very near the result from the Quad XNS tool. In Fig. 9, for example, they practically superimpose, at least out to about t = 3.3ns (t' = 1.3ns). Beyond t = 7.7nsec the XNS result exceeds even the skin effect (only) curve. However, note that this is in the "far tail" region where the response is beyond 95% of its final value, which usually is of little interest in digital systems.

Figs. 10 and 11 show the results for an open circuit 18" piece of the same 1 mil center conductor copper coax. Again, the R_{dc}*erfc curves from this analysis fall virtually on top of the Quad XNS curves out to t = 6ns and the error does not exceed about

1.25% out to 20ns. There is also a small (≈ 23ps) shift of part of the initial rise (eg., at the 50% crossing point) between the XNS and R_{dc}*erfc curves, but after t_{pd} = 3ns this is not a significant error.

Figs. 12 and 13 show similar good agreement for the 24" coax case, particularly out to t = 9.35ns. Again, however, the maximum error (aside from the small, ≈ 33ps, leading edge time difference) is only about 1.35%. For the shorter, 6" open coax case shown in Figs. 14 and 15, the agreement is excellent between our R_{dc}*erfc curve and XNS out to t = 1.35ns, but even then approximation is not bad out to t = 3ns or so. Beyond this, XNS is substantially too high, but since the response is over 95% here, the error is not important for digital applications.

1.2.6. Comment on Results

The goal of being able to calculate reasonably accurate lossy line step response curves for the simple coax line case with only standard inexpensive computational tools has been achieved. The product of the fully developed skin effect (Eq. 17) curve times the R_{dc} (only) curve (which can be adequately defined without PSpice simulation for the open circuit case by interpolating between the break points given in Eqs. 7 and 8) gives reasonable - looking results which agree very well with the XNS simulations. Probably the only way to get more accurate "proof quality" line transient response results is to carry out a frequency domain calculation as accurately as possible and then use numerical inverse Fourier transform methods to get the time domain results. Computing hardware can do Fourier transforms so quickly now that this may be an attractive approach for fully linear cases, however it does not generalize to the non-linear characteristics of many drivers and receivers of practical interest.

To briefly touch on the significance of the calculational results, rather than the methods, we can see in Figs. 7-15 that even for the open line case, line dc resistances of the order of 10Ω are important to avoid gross compromise in step response. We will be looking into the risetime and dynamic noise margin implications of these results in the future.

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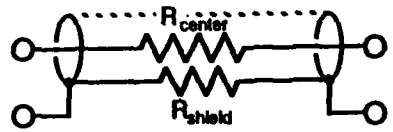
Lossy Coax dc and ac Resistance Calculation

Resistance per Unit Length, R

$R = R_{center} + R_{shield}$

$R_l = \rho / (\text{Conducting Area})$

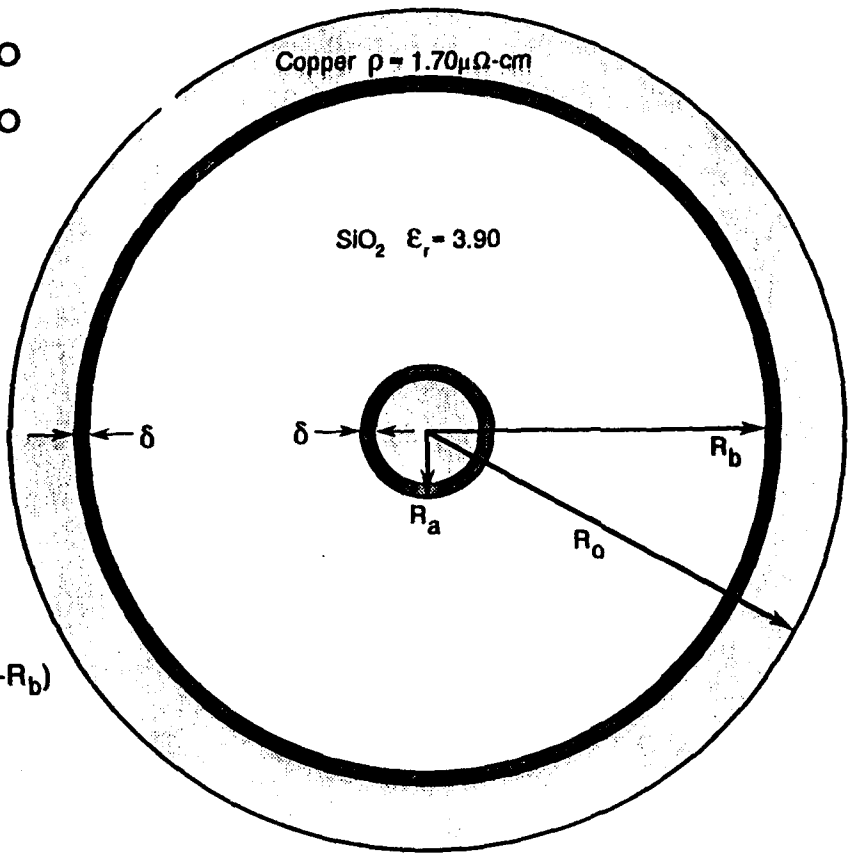


Conducting Areas:

	Center Conductor	Shield
dc:	πR_a^2	$\pi(R_o^2 - R_b^2)$
ac:	$2\pi R_a \delta$	$2\pi R_b \delta$

For $\delta < R_a$ & $(R_o - R_b)$

(δ is the ac skin effect penetration depth)



dc and ac Reststance per Unit Lengths:

$$R_{dc} = \frac{\rho}{\pi}\left(\frac{1}{R_a^2} + \frac{1}{R_o^2 - R_b^2}\right)$$

$$R_{ac}(\omega) = \text{Re}\,[R_{sel}(\omega)] = \frac{\rho}{2\pi\delta}\left(\frac{1}{R_a} + \frac{1}{R_b}\right) \leftarrow \text{For } \delta < R_a \text{ \& } (R_o - R_b)$$

Or, from 45° angle of surface impedance ($\sqrt{j\omega}$), with $\frac{\rho}{\delta} = \sqrt{\omega\mu\rho/2}$, the magnitude is just

$$|R_{sel}(\omega)| = \frac{1}{2\pi}\sqrt{\omega}\sqrt{\mu\rho}\left(\frac{1}{R_a} + \frac{1}{R_b}\right),$$

or, defining $R_s = \frac{|R_{sel}(\omega)|}{\sqrt{\omega}}$ (independent of ω), giving

$$R_s = \frac{1}{2\pi}\sqrt{\mu\rho}\left(\frac{1}{R_a} + \frac{1}{R_b}\right)$$

For line of impedance, Z_o, and length, x, skin effect time, t_{sel}, is

$t_{sel} = \left[\frac{x R_s}{4 Z_o}\right]^2$ where the R_{dc}=0 step response is $v(t) = \text{erfc}(1/\sqrt{(t - x/c')/t_{sel}})$

Figure 1

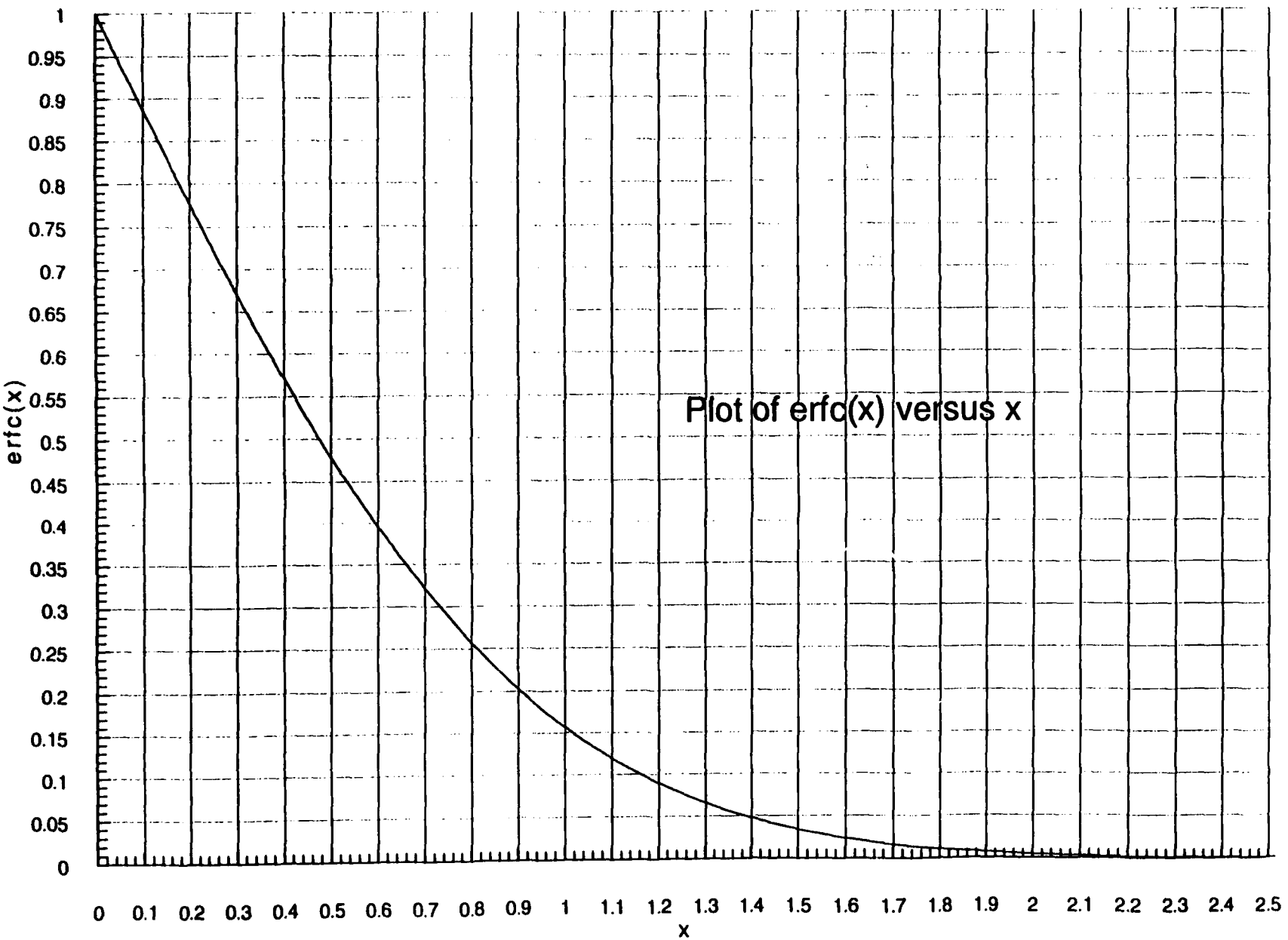

Plot of erfc(x) versus x
erfc(x)
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8 1.9 2 2.1 2.2 2.3 2.4 2.5
x

Figure 2

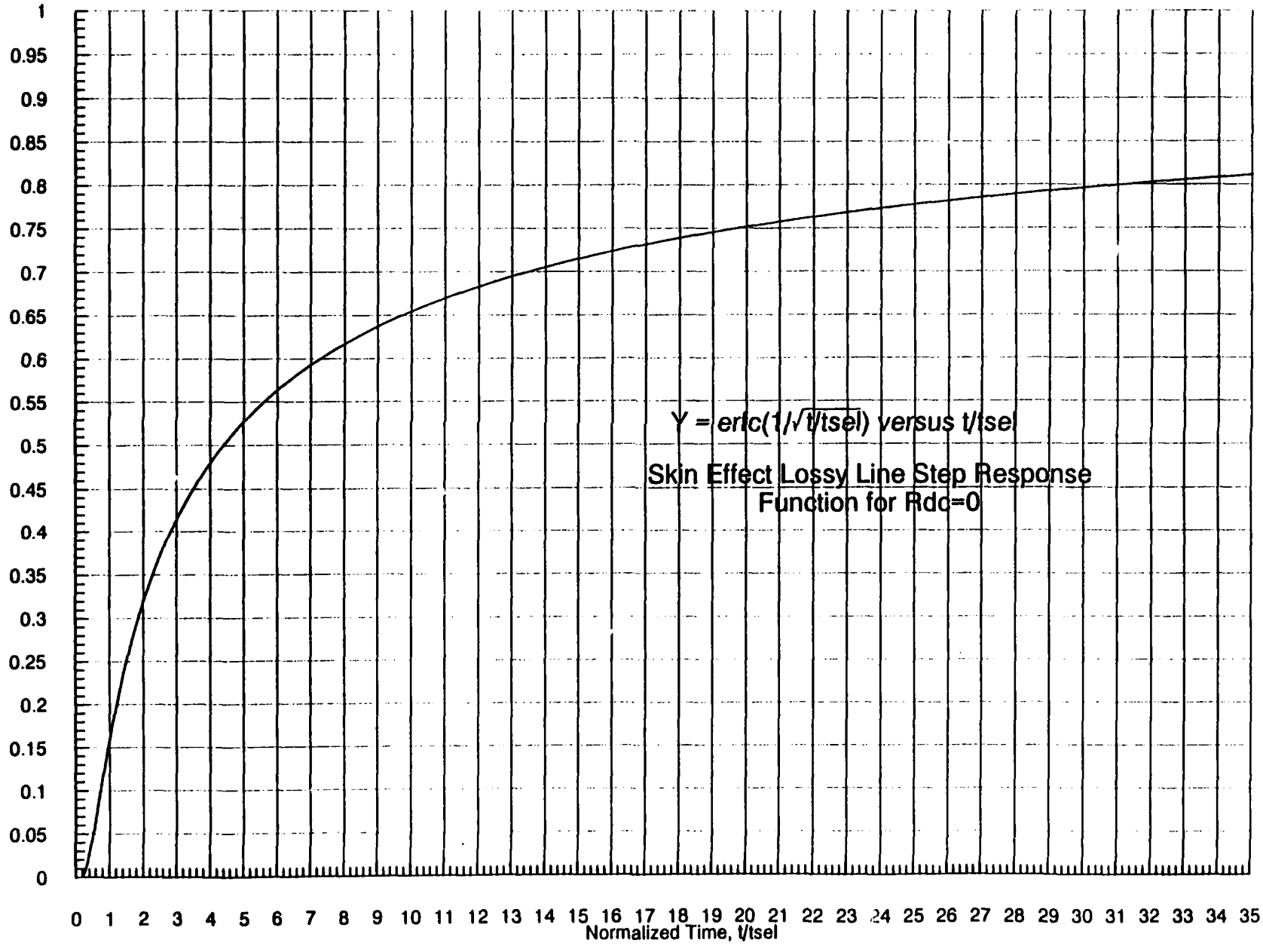

1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
Y = erfc(1/√t/tsel) versus t/tsel
Skin Effect Lossy Line Step Response
Function for Rdc=0
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
Normalized Time, t/tsel

Figure 3

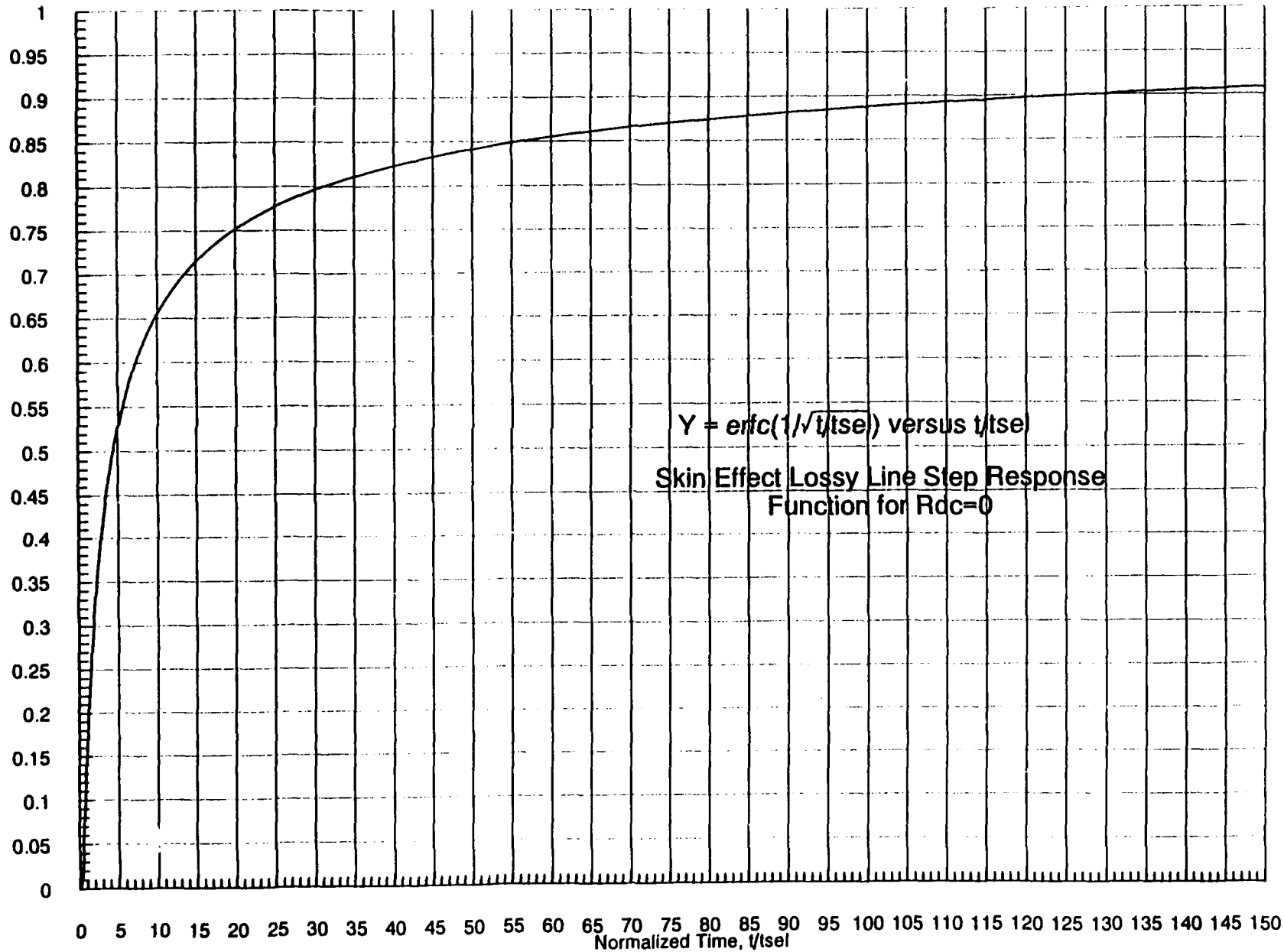

1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145 150
Normalized Time, t/tsel
Y = erfc(1/√t/tse)) versus t/tsel
Skin Effect Lossy Line Step Response
Function for Rdc=0

Figure 4

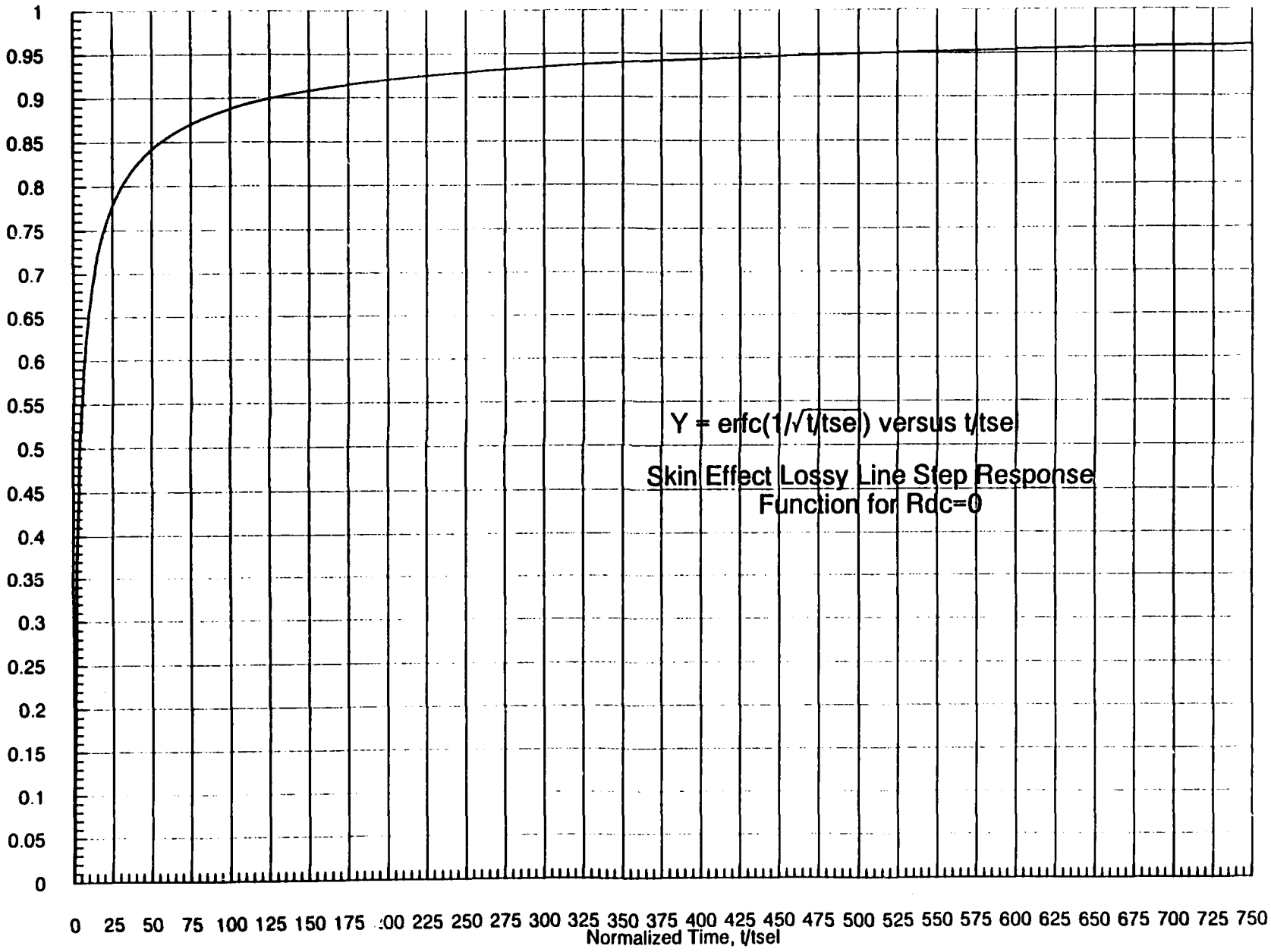

1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
Y = erfc(1/√t/tse) versus t/tse
Skin Effect Lossy Line Step Response
Function for Rdc=0
0 25 50 75 100 125 150 175 200 225 250 275 300 325 350 375 400 425 450 475 500 525 550 575 600 625 650 675 700 725 750
Normalized Time, t/tsel

Figure 5

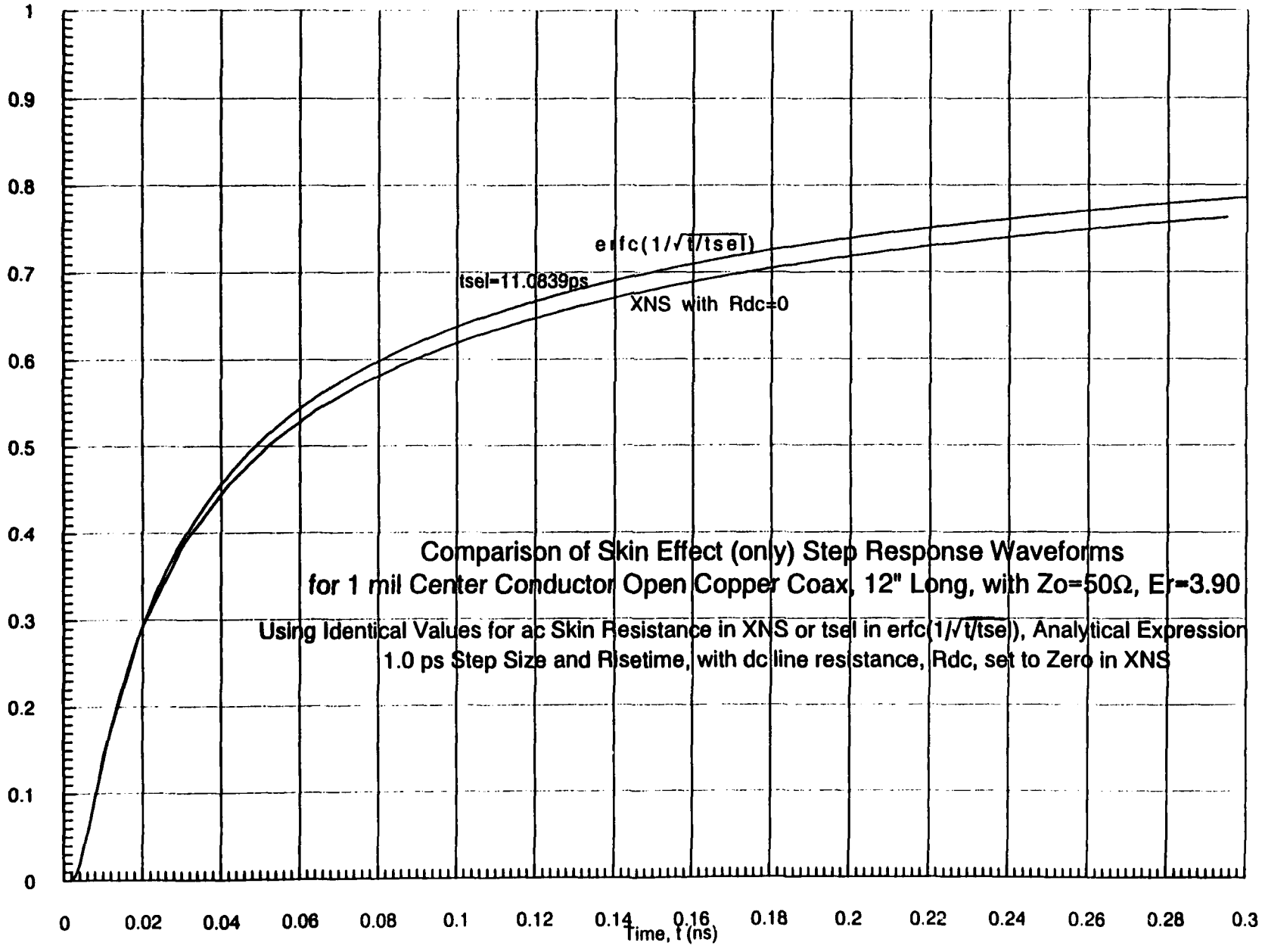

1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0.16
0.18
0.2
0.22
0.24
0.26
0.28
0.3
Time, t (ns)
erfc(1/√t/tsel)
tsel=11.0839ps
XNS with Rdc=0
Comparison of Skin Effect (only) Step Response Waveforms
for 1 mil Center Conductor Open Copper Coax, 12" Long, with Zo=50Ω, Er=3.90
Using Identical Values for ac Skin Resistance in XNS or tsel in erfc(1/√t/tse), Analytical Expression
1.0 ps Step Size and Risetime, with dc line resistance, Rdc, set to Zero in XNS

Figure 6

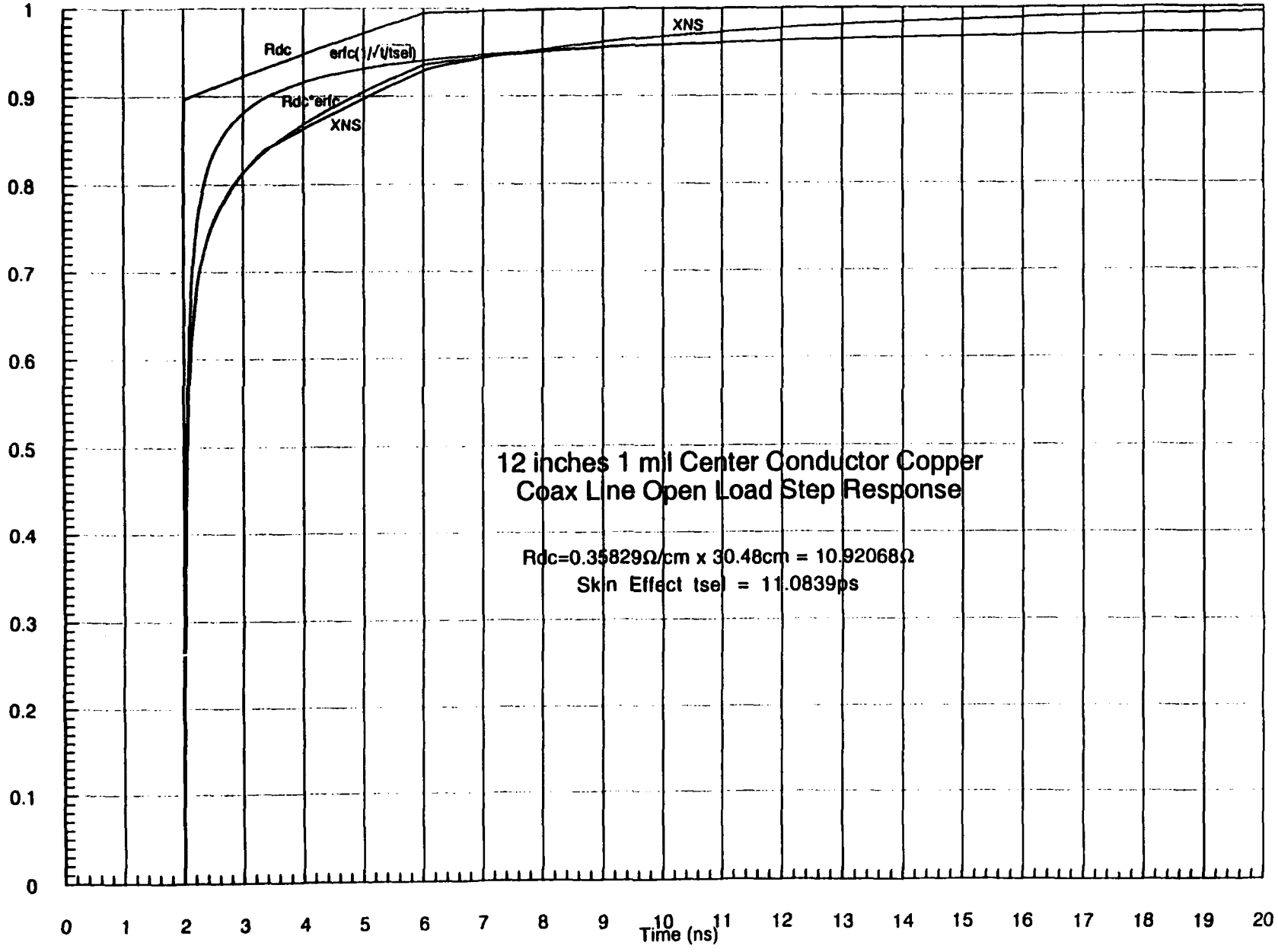

Rdc
erfc( )/√(t/tsel)
Rdc*erfc
XNS
XNS
12 inches 1 mil Center Conductor Copper
Coax Line Open Load Step Response
Rdc=0.35829Ω/cm x 30.48cm = 10.92068Ω
Skin Effect tsel = 11.0839ps
Time (ns)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

Figure 7

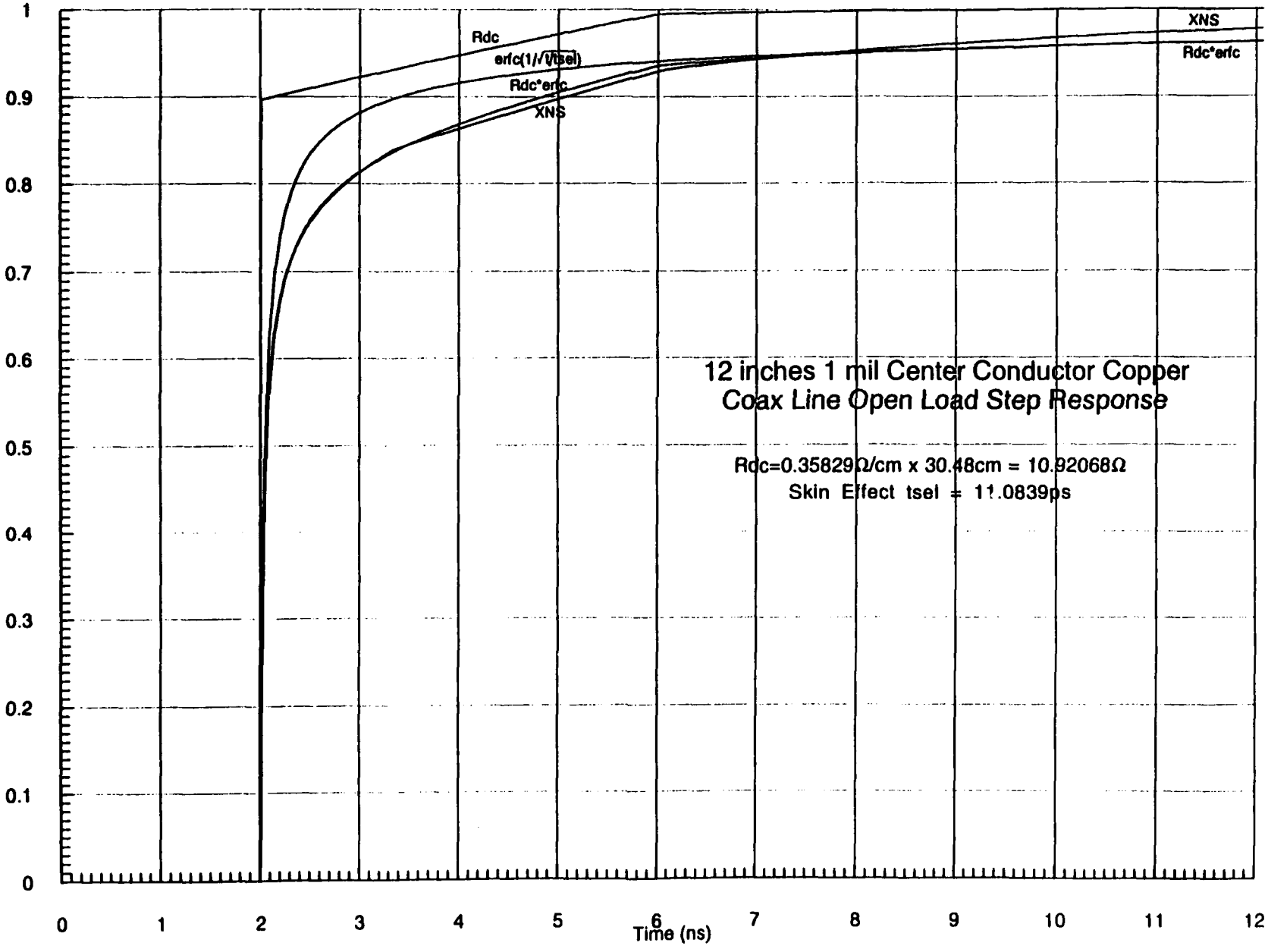

Rdc
erfc(1/√tsel)
Rdc*erfc
XNS
XNS
Rdc*erfc
12 inches 1 mil Center Conductor Copper
Coax Line Open Load Step Response
Rdc=0.35829Ω/cm x 30.48cm = 10.92068Ω
Skin Effect tsel = 11.0839ps
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
1
2
3
4
5
6
7
8
9
10
11
12
Time (ns)

Figure 8

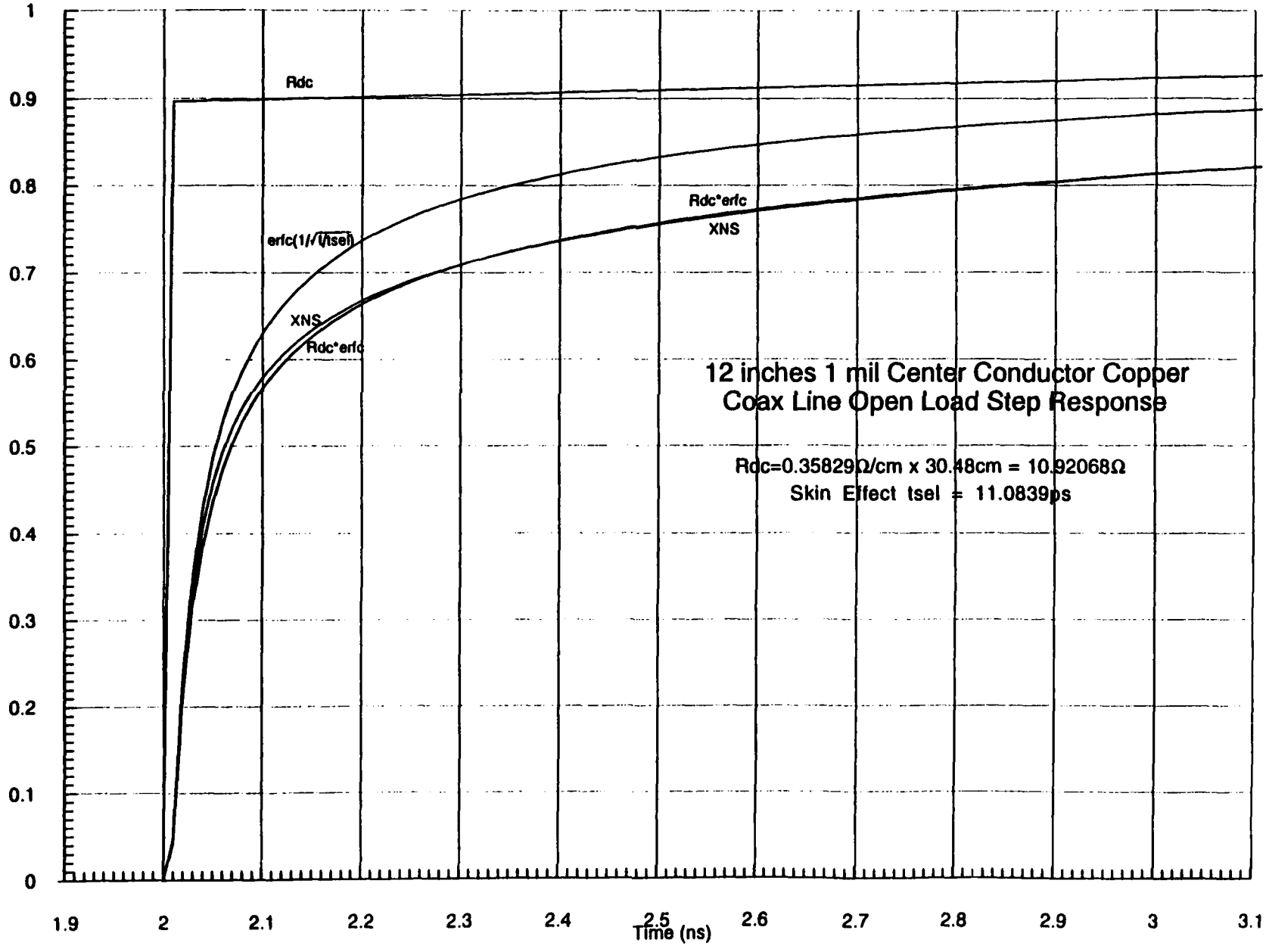

Rdc
erfc(1/√(tsel))
XNS
Rdc*erfc
Rdc*erfc
XNS
12 inches 1 mil Center Conductor Copper
Coax Line Open Load Step Response
Rdc=0.35829Ω/cm x 30.48cm = 10.92068Ω
Skin Effect tsel = 11.0839ps
Time (ns)
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
1.9
2
2.1
2.2
2.3
2.4
2.5
2.6
2.7
2.8
2.9
3
3.1

Figure 9

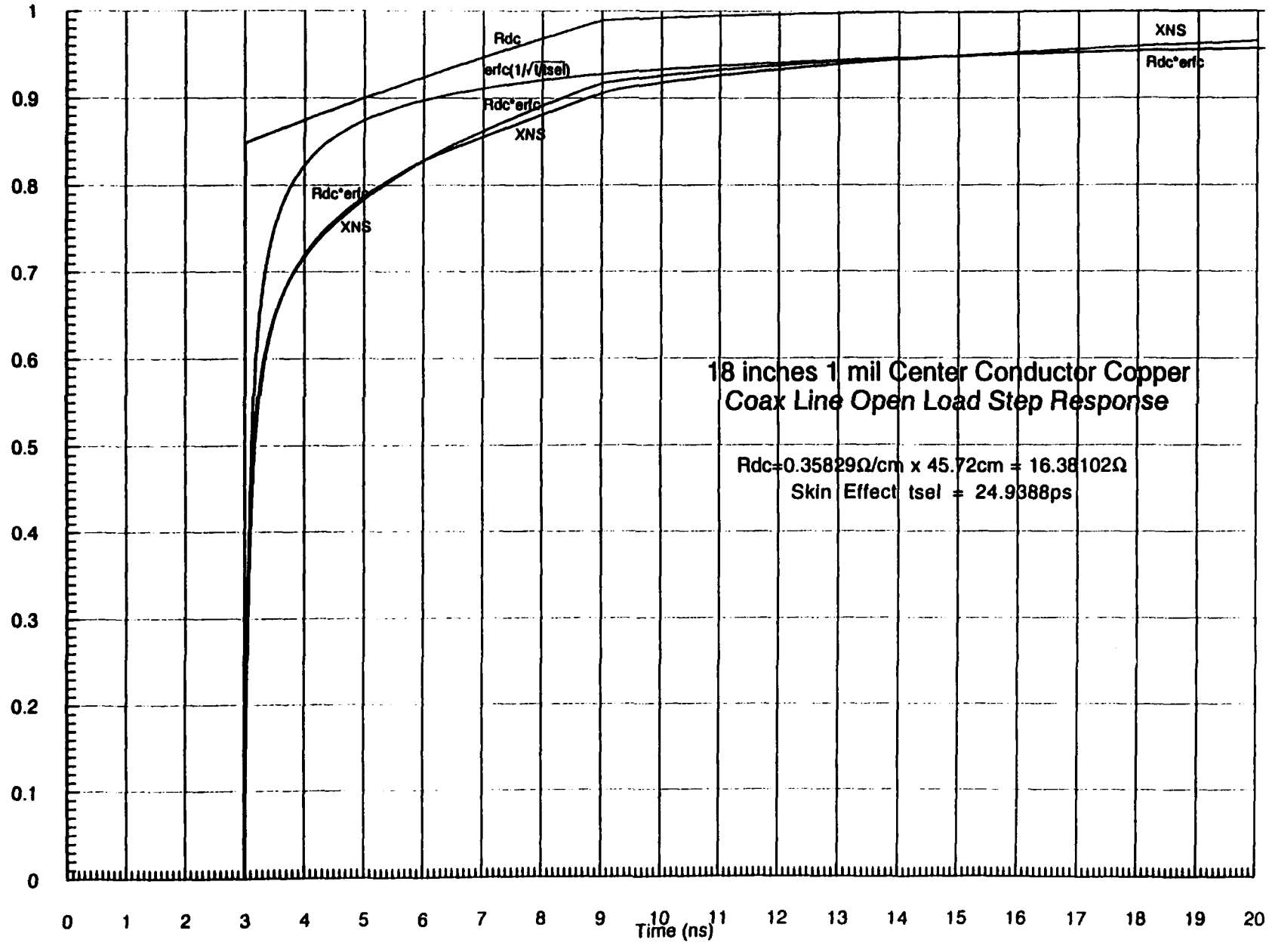

1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Time (ns)
Rdc
erfc(1/√tsel)
Rdc*erfc
XNS
Rdc*erfc
XNS
XNS
Rdc*erfc
18 inches 1 mil Center Conductor Copper
Coax Line Open Load Step Response
Rdc=0.35829Ω/cm x 45.72cm = 16.38102Ω
Skin Effect tsel = 24.9388ps

Figure 10

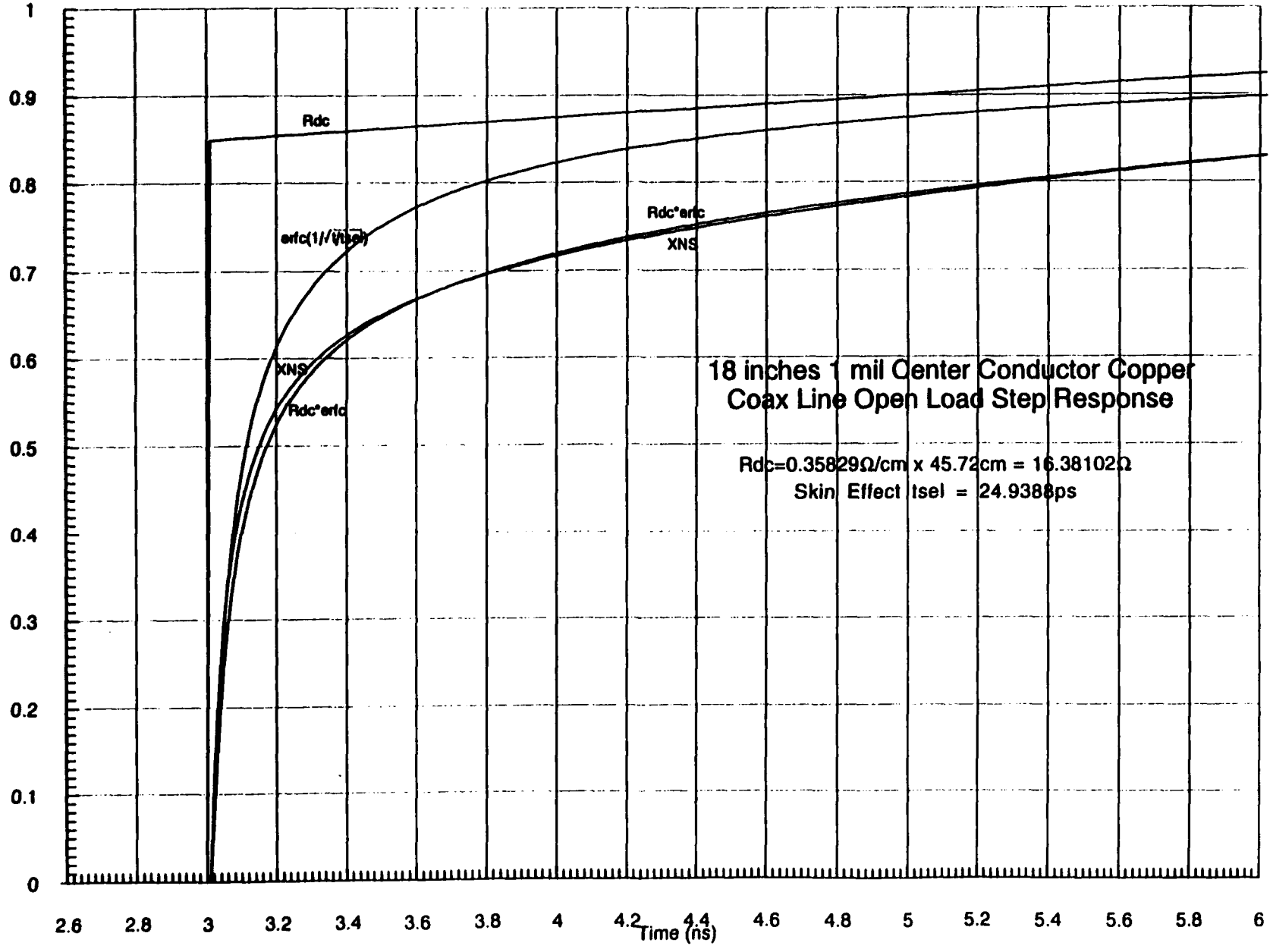

1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Rdc
erfc(1/√(t/tsel))
XNS
Rdc*erfc
Rdc*erfc
XNS
18 inches 1 mil Center Conductor Copper
Coax Line Open Load Step Response
Rdc=0.35829Ω/cm x 45.72cm = 16.38102Ω
Skin Effect tsel = 24.9388ps
2.6
2.8
3
3.2
3.4
3.6
3.8
4
4.2
4.4
4.6
4.8
5
5.2
5.4
5.6
5.8
6
Time (ns)

Figure 11

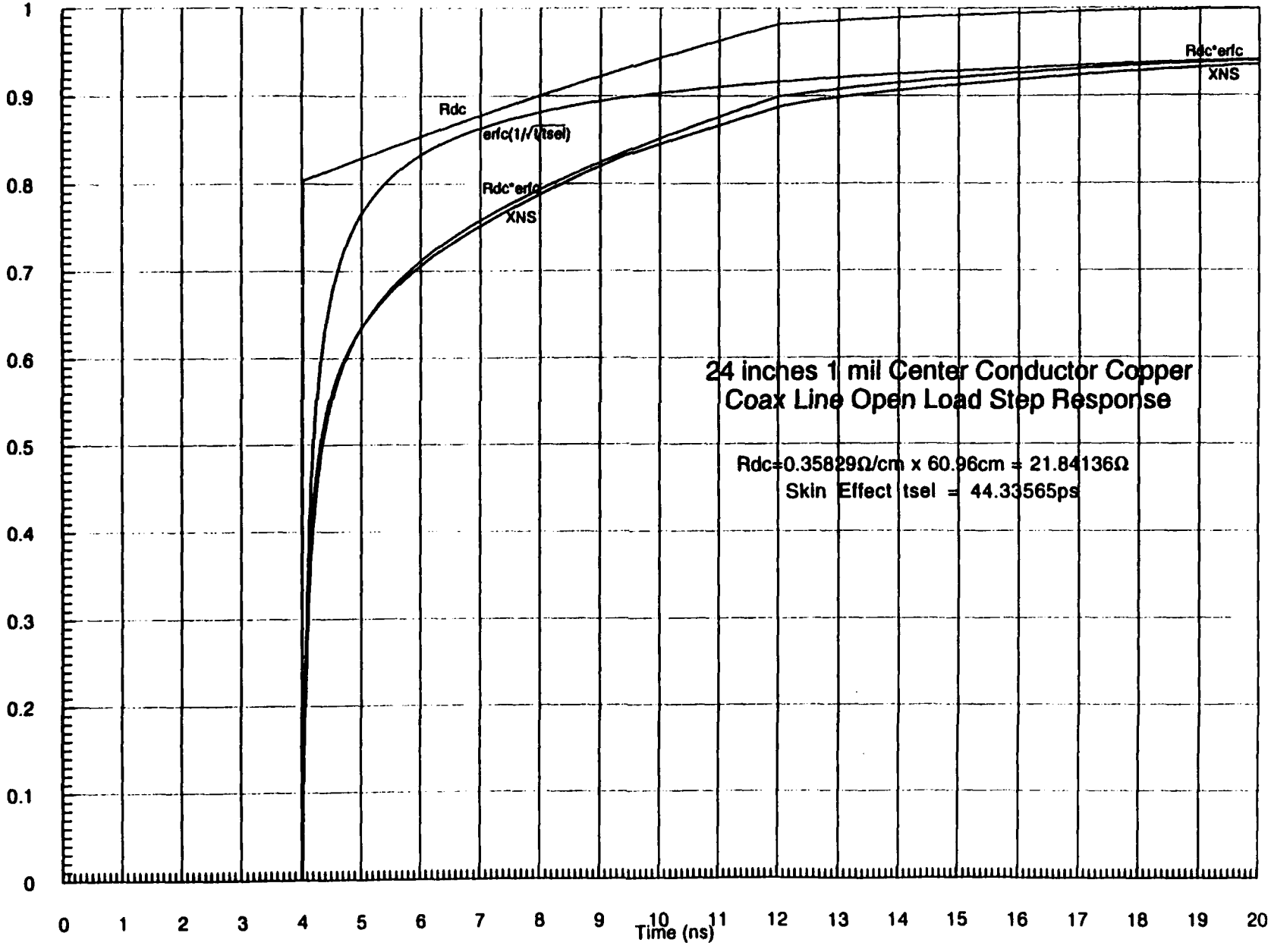

1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Time (ns)
Rdc
erfc(1/√tsel)
Rdc*erfc
XNS
Rdc*erfc
XNS
24 inches 1 mil Center Conductor Copper
Coax Line Open Load Step Response
Rdc=0.35829Ω/cm x 60.96cm = 21.84136Ω
Skin Effect tsel = 44.33565ps

Figure 12

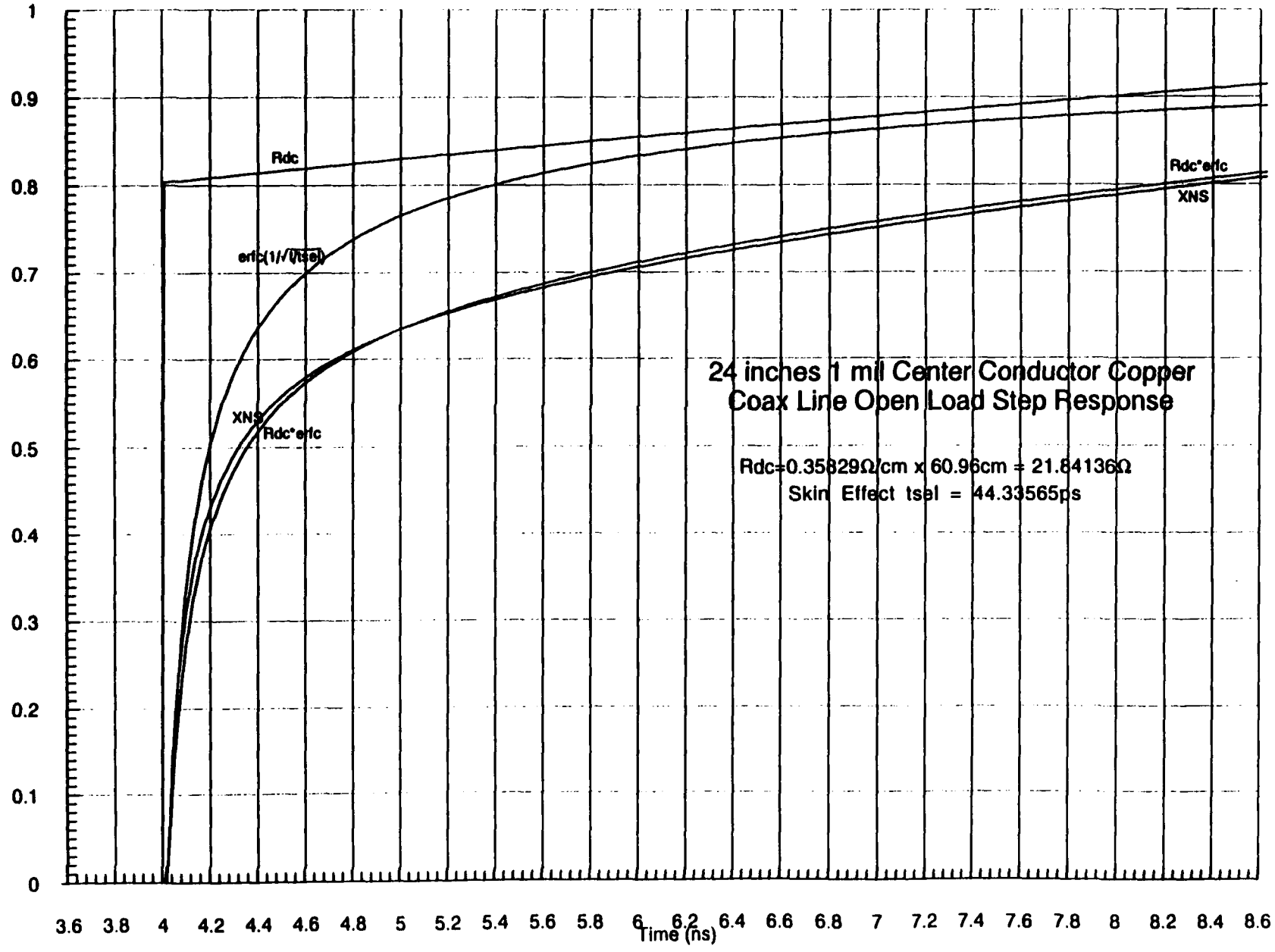

24 inches 1 mil Center Conductor Copper
Coax Line Open Load Step Response
Rdc=0.35829Ω/cm x 60.96cm = 21.84136Ω
Skin Effect tsel = 44.33565ps
Rdc
erfc(1/√(t/tsel))
XNS
Rdc*erfc
Rdc*erfc
XNS
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
3.6 3.8 4 4.2 4.4 4.6 4.8 5 5.2 5.4 5.6 5.8 6 6.2 6.4 6.6 6.8 7 7.2 7.4 7.6 7.8 8 8.2 8.4 8.6
Time (ns)

Figure 13

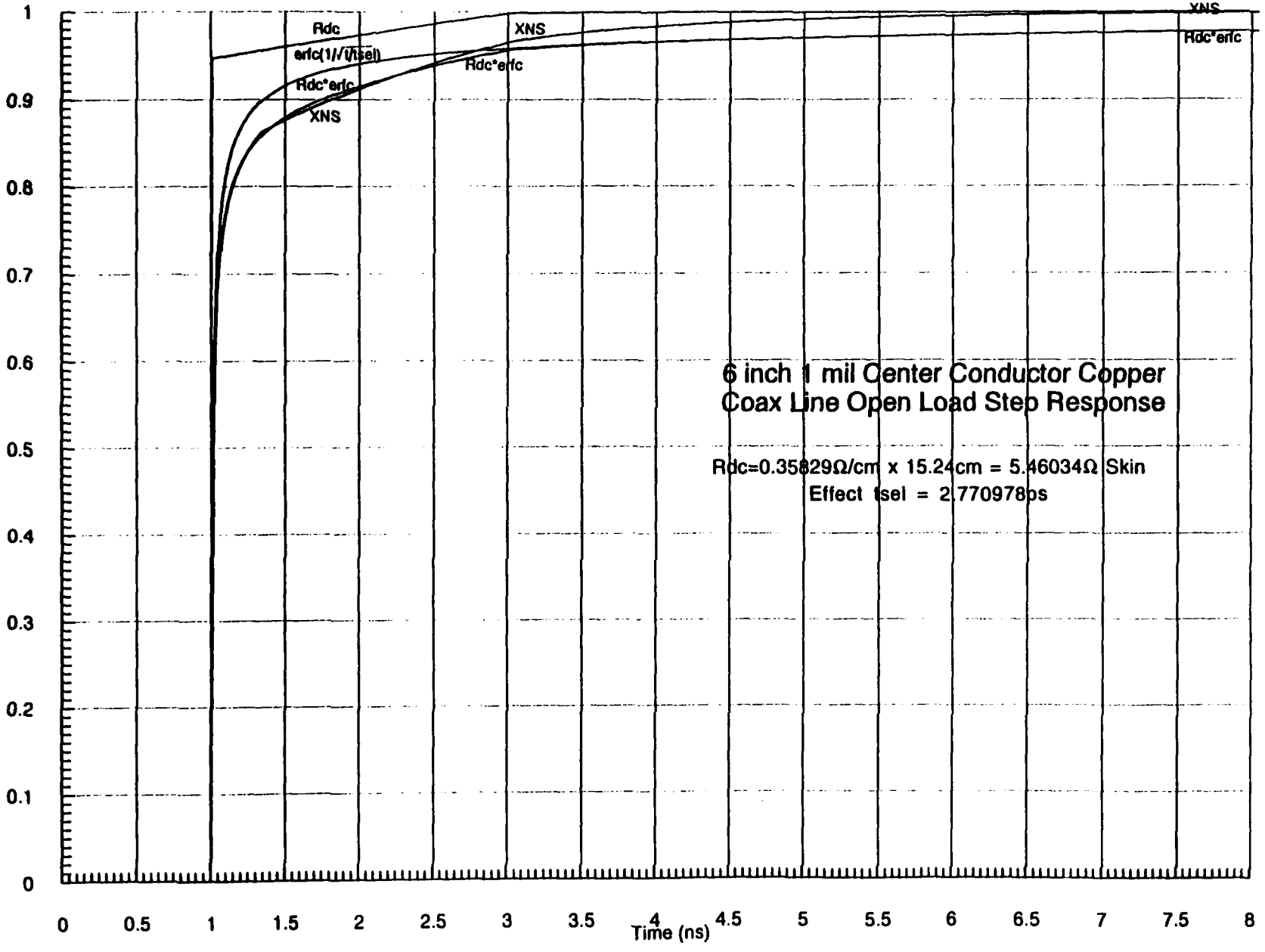

Rdc
erfc(1/√tsel)
Rdc*erfc
XNS
XNS
Rdc*erfc
XNS
Rdc*erfc
6 inch 1 mil Center Conductor Copper
Coax Line Open Load Step Response
Rdc=0.35829Ω/cm x 15.24cm = 5.46034Ω Skin
Effect tsel = 2.770978ps
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
5.5
6
6.5
7
7.5
8
Time (ns)

Figure 14

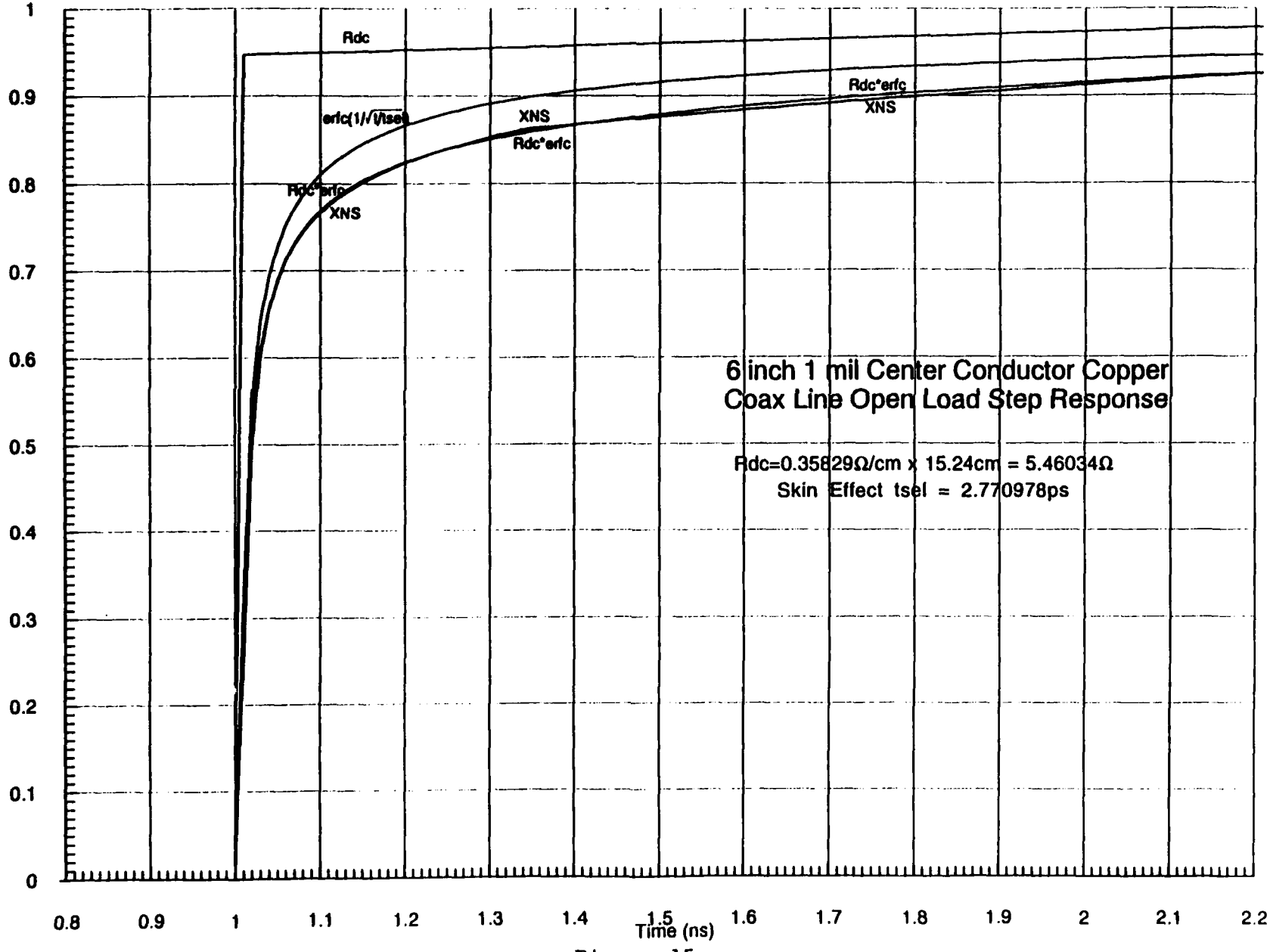

Rdc
erfc(1/√tsel)
XNS
Rdc*erfc
Rdc*erfc
XNS
Rdc*erfc
XNS
6 inch 1 mil Center Conductor Copper
Coax Line Open Load Step Response
Rdc=0.35829Ω/cm x 15.24cm = 5.46034Ω
Skin Effect tsel = 2.770978ps
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.9
1
1.1
1.2
1.3
1.4
1.5
1.6
1.7
1.8
1.9
2
2.1
2.2
Time (ns)

Figure 15

Section 2.0

Commercialization of High Temperature Superconducting Technology

2.1. Background

During this quarter, emphasis was put on cryoelectronic technology market development issues. In earlier reports we discussed the significance of this technology to the commercial and defense sectors. What we attempted to do in this quarter is to better understand the cryoinfrastructure. Specifically, what product/service would a cryoelectronic company provide to survive. It is clear that the semiconductor houses recognize the performance increase gained by CMOS as it is chilled. It is also recognized by system houses that chilled CMOS system could yield factor of two or higher in system performance. So the question is what would it take to get this technology to be accepted by the industry. Recent cost reduction and performance improvement in cryogenics indicate that this part of the cryoelectronics may not be the long pole in the tent. Furthermore, the next generation of CMOS foundries indeed will cost nearly one billion dollars. So it would seem a major near term leap frog can take place if the various pieces of the technology can be brought together and particularly if the cryopart can be transparent to the system designer. Obviously, it is difficult to educate, at least in the near term, many system houses on how to use cryogenics. However, there are companies such as STI and Conductus which already have cryolectronic know how, due to their experience in superconductivity. These companies however do not have much experience in the digital industry.

Our job has been to work with them to help orient to the right market niche. It seems that there is room for a business which supplies a system solution to those system houses intending to use cryoelectronics. That includes device optimization, CAE-tools, packaging, integration and assembly as well as testing. Another business niche may be to work with workstation houses to take current and next generation products and optimize for cryoapplication using some architecture. Although only a few days have been spent in this area, we believe significantly greater time is needed with these people to get the IC industry moving. Potentially new generations of workstations can be realized within a relatively short term without having to wait for the emergence of next generation CMOS.

3.3 Q2 1992 Quarterly Report

Section 1.0

Transient Response Characteristics of Small MCM Interconnect Lines, Including Complex, Frequency Dependent Characteristic Impedance Effects

1.1. Background

As discussed in the background for the last quarterly report, the critical driving force toward the use of high temperature superconducting (HTSC) interconnect lines in large, maximal density multi-chip modules (MCMs) is line resistance. Adequately small end to end ohmic line resistances (much smaller than the characteristic impedance, Z_o) are only achievable with normal metal interconnects by making the conductors quite large ($\sim$1mil for room temperature copper). These large conductor diameters (or widths for stripline or microstrip conductors) severely limit the number of interconnections which can be completed on each layer, and hence require excessive and impractical numbers of signal layers to implement large, maximal density MCMs (see references 5 and 6).

The impetus to develop HTSC MCM technology, then, is a fairly quantitative issue, depending quite specifically on just what conductor dc and ac (skin effect) resistance levels are tolerable in digital MCM interconnect applications. The last quarterly report (Eqs. 1-24, Figs. 1-15, References 1-4 and associated text, Sections 1.1-1.2.6) addressed analytical approximations which allow estimates of the transient response of normal metal interconnect lines to be generated with minimal computational effort, and compared the results for the specific case of small coaxial lines to those generated by the Quad Design XTK suite of commercial CAE tools. It was noted in that report that both the analytic methods and the commercial CAE tools involve significant approximations (in order to keep run times acceptable in an engineering environment for the commercial tools), which have noticeable impact on the

accuracy of the results. In particular, substantial differences were seen between the methods explored in the "tail" region of the rise characteristic, particularly above 90% to 95% of the final value, even though the basic assumptions behind the calculations were the same. Fortunately, the 20% to 80% or 10% to 90% regions of the signal waveforms are of the greatest interest in most digital MCM or PCB applications, so this is not a serious concern in a commercial CAE environment. However, for mixed mode MCM applications, more detailed transmission line characterization could be required, and in any event, it would be comforting to know what really is the true lossy line transient response, in order to evaluate the impact of the various approximations necessary to facilitate the "practical" solutions discussed in the previous report.

This report, then, simply picks up where the previous report stops. Hence, in order to avoid endless usage of "equation or reference number (x) of the previous report", we will simply continue the numbering of equations (starting here at Eq. 25), Figures (starting here at Fig. 16), and References (starting here at Ref. 5) from where the last report stopped.

1.2. Non - Approximate Forms of Basic Lossy Transmission Line Equations

The basic approach to the lossy transmission line problem discussed in the last quarterly report (Eqs. 1-24, Figs. 1-15 and Refs. 1-4) is the perturbation method (see section 4.6 of Ref. 2), with the assumption of small losses such that, for lossless dielectrics (only conductor losses), the complex propagation constant, is given by

$$\gamma + \alpha + j\beta \approx j\omega \sqrt{LC} + \frac{R}{2}\sqrt{\frac{C}{L}} \qquad \text{Eq. 25}$$

and characteristic impedance, Z_o, by

$$Z_o \approx \sqrt{\frac{L}{C}} \qquad \text{Eq. 26}$$

These are approximations to the general expressions for lossless dielectrics/lossy conductor lines for the complex propagation constant

$$\gamma = \sqrt{j\omega C\,(R + j\omega L)} \qquad \text{Eq. 27}$$

and the complex characteristic impedance

$$Z_o = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{j\omega C}} \qquad \text{Eq. 28}$$

For completeness (for the benefit of those for whom a few years may have passed since their last transmission line course), the frequency dependent, complex propagation constant, γ, is used in the voltage and current propagation equations

$$V(z) = V_o^+ e^{-\gamma x} + V_o^- e^{+\gamma x} \qquad \text{Eq. 29}$$

and

$$I(z) = I_o^+ e^{-\gamma x} + I_o^- e^{+\gamma x} \qquad \text{Eq. 30}$$

where the + and - superscripts correspond to propagation in the $+x$ and $-x$ directions, and the complex, frequency dependent characteristic impedance, Z_o, is defined by

$$Z_o = \frac{V_o^+}{I_o^+} = \frac{-V_o^-}{I_o^-} \qquad \text{Eq. 31}$$

As noted in section 1.2.3 of the last report (Equations 9-23), the low loss assumptions of Eq. 25 and 26, taken along with the assumption of pure skin effect loss ($R_{dc} = 0$), allows the frequency domain signal propagation expression to be analytically Fourier transformed back to the time domain, giving the erfc function step response solution (Eqs. 14-19). Analytic Fourier transforms are not available to convert frequency - domain results calculated using the general lossy line equations (Eq. 27 and 28), particularly when both dc and ac (skin effect) line resistance contribution are included. Hence, the strategy utilized here is to avoid the use of approximations, solving in the frequency domain the general transmission line equations with complex, frequency dependant γ and Z_o and then using numerical techniques to transform the results back into the time domain. While this technique can always be used to model the linear elements (successions of transmission line segments, boundary shunt impedances, etc) in a problem, we will go ahead and assume that the voltage generator (V_{in}) source impedance, and the Z_{in}, load impedance, Z_2, are also linear. This allows us to solve the entire problem in the frequency domain and do a single inverse Fourier transform (iFFT) to get the result (as opposed to XNS, which allows nonlinear drivers and loads by using the impulse response of the line segments in a discrete time simulation of the circuit).

The problem solved is illustrated in Fig. 16. Since almost all of the variables are complex frequency dependent values (eg., γ, Z_o, Z_1, Z_2, Z_{in}, and all *V's* and *I's*), for simplicity in notation they will not be specially marked to show this. (It is fairly clear that the quantities such as *R's, L's, C's* and distances such as x or l are scalars). Treated is a voltage generator, V_{in}, with source impedance, Z_{in}, connected through a single lossy transmission line segment of characteristic impedance Z_o and length l, to a load, Z_2. The unknowns are the voltages at both ends of the line, V_1 at the source end and V_2 at the load (frequently we are most interested in the load voltage, V_2, but this necessitates first finding V_1). Numerically, of course, the solution is carried out for all frequencies before carrying out the iFFT to get the time domain solution.

The approach to the frequency domain solution is illustrated in Fig. 16. First, the load impedance, Z_2, is transformed back to an equivalent impedance, Z_1, located at the source side of the line, using the general transmission line equations (Eqs. 27-31). A bit of messy complex arithmetic is saved by the fact that these transformations were done may decades ago and are published in many standard handbooks (see, for example, Ref. 7). This Z_2 to Z_1 impedance transform through length x is just

$$\frac{Z_1}{Z_o} = \frac{Z_2 \cosh(\gamma x) + Z_o \sinh(\gamma x)}{Z_o \cosh(\gamma x) + Z_2 \sinh(\gamma x)} \qquad \text{Eq. 32}$$

where for our case, $x = l$. One of the cases of interest is for an open circuit line ($Z_2 = \infty$), in which case Eq. 32 becomes

$$\frac{Z_1}{Z_o} = \coth(\gamma x) \qquad \text{for } Z_2 \text{ open} \qquad \text{Eq. 33}$$

Having transformed the load impedance, Z_2, back to an equivalent Z_1 at the source, we can use the simple voltage divider equation to obtain the voltage V_1 at the source end of the line as

$$V_1 = V_{in} \left[\frac{Z_1}{Z_{in} + Z_1} \right] \qquad \text{Eq. 34}$$

or, $V_1 = V_{in}$ if Z_1 happens to be infinite, such as for an open circuit line at dc (f = 0). To get the voltage at the load end of the line, V_2, having calculated the voltage at the source end, V_1, from Eq. 34, we simply use the transform

$$\frac{V_2}{V_1} = \frac{1}{\cosh(\gamma x) + (Z_o/Z_2)\sinh(\gamma x)} \qquad \text{Eq. 35}$$

We can use the iFFT operation to go from the frequency domain V_2 to obtain the time domain output, $V_2(t)$.

It should be noted at this point that while the frequency domain solutions based on Eqs. 27, 28 and 32-35 are deceivingly simple and concise, they involve complex functions (sinh, cosh, coth, sqrt, etc.) of complex arguments, which would be a bit of a chore to deal with if the programming language doesn't support complex variables and have the requisite functions in its library. For this work, the program "HiQ" from Bimillennium Corp., 101 Albright Way, Los Gatos, CA 95030, (800) 488-8662, running on either a Mackintosh IIfx or a Powerbook 170 was used for calculations and most graphics output. Presumably, Mathematica would also work for this.

1.3. Coaxial Line Frequency Dependance of Resistance and Inductance - Kelvin Function Solutions

As was discussed in section 1.2.2, because even fast rise time step signal require low frequency components to accurately represent them (frequencies for which the skin effect depths will typically exceed the conductor dimensions), both the dc (R_{dc}) and the skin effect (R_s) losses must be included to obtain accurate results for real lossy lines. This creates one problem in that the inverse Fourier transform to convert lossy line frequency response to time domain transient response, which is known in closed analytic form for the fully developed skin effect case (Eqs. 14-18), is not known in closed analytic form for the mixed R_{dc} + skin effect case. We are getting around that problem by using numerical methods for taking the iFFT to obtain the time domain response. Unfortunately, in general, even the frequency domain response is not well known in the "crossover" region between low frequencies (where R_{dc} dominates) and high frequencies (where R_s dominates), (ie., where the skin effect depth [δ in Eq. 2] is comparable to the conductor dimensions). In Section 2.4 of Ref. 5, approximate analytic expression for the frequency dependence for microstrip and stripline conductor geometries were developed which would be very helpful for use with numerical methods for obtaining the inverse Fourier transform (IFT) to get the time domain response for these conductor geometries.

Fortunately, the frequency dependence of the ac resistance, R_{ac}, and internal inductance, L_{int}, of the round wire center conductor in coax are known analytically as a function of frequency for frequencies from dc, where Eq. 5 is valid, up to the region where the high frequency approximation of Fig. 1 or Eqs. 9 and 10 becomes valid (eq., the skin depth δ [Eq. 2] becomes much less than the center conductor radius, R_a). In the example of a 50Ω coax with ε_r = 3.90 dielectric constant, the shield inner radius, R_b, is 5.19055572 times the center conductor radius, and hence the shield contributions to R_{ac} and L_{int} are only 16% of the total. Hence, it will be fairly accurate if we simply scale the results for the center conductor by the factor $[1 + R_a/R_b]$, that is:

$$R_{ac}(coax) \approx R_{ac}(\text{center conductor}) \left[1 + \frac{R_a}{R_b}\right] \qquad \text{Eq. 36}$$

and

$$L_{int}(\text{coax}) \approx L_{int}(\text{center conductor}) \left[1 + \frac{R_a}{R_b}\right] \qquad \text{Eq. 37}$$

As noted in Fig. 1, the dc resistance (per meter) of the center conductor is given by

$$R_{dc}(c.c.) = \rho / \left(\pi R_a^2\right) \qquad \text{Eq. 38}$$

and its dc internal inductance by Eq. 5. The frequency dependence of the internal inductance and ac resistance of the center conductor is carried out in terms of the dimensionless ratio, ζ, between the center conductor radius, R_a, and the (frequency dependant) skin depth, δ, as (Ref. 2)

$$\zeta = \sqrt{2}\ R_a/\delta \qquad \text{Eq. 39}$$

As described in Section 4.5.3 of Ref. 2 (Gardial), the real and imaginary parts of the center conductor impedance per unit length are given by

$$R_{ac}(c.c) = R_{dc}(c.c) \left(\frac{\zeta}{2}\right) \frac{[ber(\zeta)\ bei'(\zeta) - bei(\zeta)\ ber'(\zeta)]}{[bei'(\zeta)]^2 + [ber'(\zeta)]^2} \qquad \text{Eq. 40}$$

and

$$L_{int}(c.c) = L_{int\ dc}(c.c) \left(\frac{4}{\zeta}\right) \frac{[bei(\zeta)\ bei'(\zeta) + ber(\zeta)\ ber'(\zeta)]}{[bei'(\zeta)]^2 + [ber'(\zeta)]^2} \qquad \text{Eq. 41}$$

where $L_{int\,dc} = \mu_o / 8\pi$ as given in Eq. 5. The functions *ber*(ζ) and *bei*(ζ) are the Kelvin functions (Ref. 8), which are the real and imaginary parts of complex Bessel functions. In the HiQ program these zero order Kelvin functions are called respectively as *ber* (0,zeta) and *bei* (0,zeta). The primes indicate first derivatives with respect to ζ , which numerically was executed with a 3-point derivative with a step size of 0.02.

Fig. 17 shows a plot of R_{ac} (coax) and L_{int} (coax) for the 1 mil center conductor, $\varepsilon_r = 3.90$, nominal $Z_o = 50\Omega$ coax [with room temperature copper ($\rho = 1.70\mu\Omega/cm$) center conductor and shield], example, calculated using Eqs. 36-41. Note that in the "skin effect only" ($R_{dc} = 0$) approximation of Eqs. 9 and 10, the R_{ac} curve goes to zero at $f = 0$ and L_{int} approaches infinity as the frequency, f, approaches zero. The Kelvin function calculated curves in Fig. 17 appear to exhibit the proper behavior and values.

One practical problem in using the Kelvin function solutions is that these complex functions end up being evaluated eight times (4 *ber* and 4 *bei*) for each frequency point (to give the functional values and 3-point derivative values), which is a great deal more computational effort than the simple approximate expressions of Eqs. 9 and 10. Further, at very high frequencies (where ζ can get very large), the numerical accuracy of the functional evaluations could become questionable (particularly the derivatives). To solve both problems, simple analytical approximations to these *ber /bei* expressions were developed. The function to be approximated for R_{ac} evaluation purposes, *RacBer* is given by

$$RacBer\,(\zeta) = \frac{[ber\,(\zeta)\;bei'(\zeta) - bei\,(\zeta)\;ber'(\zeta)]}{[bei'(\zeta)]^2 + [ber'(\zeta)]^2} \qquad \text{Eq. 42}$$

and the function for L_{int} evaluation is

$$LintBer\,(\zeta) = \frac{[ber\,(\zeta)\;bei\,'(\zeta) + bei\,(\zeta)\;ber'\,(\zeta)]}{[bei'\,(\zeta)]^2 + [ber'\,(\zeta)]^2} \qquad \text{Eq. 43}$$

Both of these functions approach the value of $1/\sqrt{2}$ for very large values of ζ. Figure 18 shows the basis for the simple approximation for $RacBer\,(\zeta)$ for ζ large:

$$RacBer\,(\zeta) \cong \frac{1}{\sqrt{2}} + \frac{0.5011275}{(\zeta - 0.475)} \text{ for } \zeta > 10 \qquad \text{Eq. 44}$$

This approximation is accurate to about 1 part in 10^5 for $\zeta > 10$, and 0.02% for $\zeta > 5$. The approximation for $LintBer\,\zeta$ is illustrated in Fig. 19:

$$LintBer\,(\zeta) = \frac{1}{\sqrt{2}} - \frac{0.5156}{(\zeta - 0.677)^2} \text{ for } \zeta > 10 \qquad \text{Eq. 45}$$

This approximation is accurate to about 2 parts in 10^6 for $\zeta > 10$ and about 0.02% for $\zeta > 6$. Fig. 20 compares the actual *RacBer* and *LintBer* functions of Eq. 42 and 43 (points) with these approximate forms of Eqs. 44 and 45 (solid curves).

1.4. Frequency Dependence of (Complex) Characteristic Impedance of Small Copper Coax Lines

The coaxial line capacitance per meter, C (Eq. 3), and inductance external to the conductors themselves, L_{ext} (Eq. 1) are used to calculate the nominal characteristic impedance, Z_o (nominal) of the line (Eq. 4) from $Z_o = \sqrt{L_{ext}/C}$. At high frequencies, where the skin depth is very small in comparison to the conductor dimensions, the actual characteristic impedance approaches this nominal value. In general, however, the inductance is larger than L_{ext} by the amount of the inductance due to magnetic fields within the conductors themselves, L_{int}, that is,

$$L = L_{ext} + L_{int} \qquad \text{Eq. 46}$$

In the numerical frequency domain calculations, the L_{int} value from Eqs. 41 and 37 (using Eq. 45 for $\zeta > 10$) is added to L_{ext} (Eq. 1 to give the total L value to go into Eqs. 28 (for Z_o) and 27 (for γ). Similarly, the R_{ac} value from Eq. 40 (with Eq. 44 for $\zeta > 10$) is used in Eq. 36 to include the shield loss, and that R_{ac} (coax) value goes in for R in Eqs. 27 and 28, along with the C value from Eq. 3 to calculate the complex, frequency dependent γ and Z_o values.

Fig. 21 shows the results for the complex characteristic impedance for the 1 mil center conductor copper coax example for frequencies from 10MHz to 5GHz. The characteristic impedance is $Z_o = 65.68\Omega - j\,36.9\Omega$ at 10MHz, $Z_o = 58.23\Omega - j\,21.0\Omega$ at 20MHz, $Z_o = 55.0\Omega - j\,9.4\Omega$ at 50MHz and drops to $Z_o = 54.13\Omega - j\,5.53\Omega$ at 100MHz, still over 8% above its nominal Z_o (nominal) = 50.00Ω value. At 1GHz, $Z_o = 51.473\Omega - j\,1.56\Omega$ fairly close to nominal. For smaller conductor sizes, as seen in Fig. 22 for the case of a 1/2 mil diameter center conductor coax (all dimensions 2x smaller than the 1 mil case, so Z_o (nominal) still is 50.00Ω), the effect is more dramatic.

For the 1/2 mil copper coax, $Z_o = 106.1\Omega - j\,91.13\Omega$ at 10MHz, $Z_o = 80.83\Omega - j\,59.84\Omega$ at 20MHz, $Z_o = 62.57\Omega - j\,31.0\Omega$ at 50MHz and $Z_o = 57.0\Omega - j\,17.3\Omega$ at f = 100MHz ($|Z_o| = 59.54\Omega$ is still nearly 20% above nominal at 100MHz). Even at 1GHz, $Z_o = 52.9 - j\,3.3\Omega$, $|Z_o| = 53.0\Omega$ is 6% above nominal. Considering that most analysis methods assume Z_o to be constant, it is clear that problems should be expected for these for small line dimensions.

1.5. Frequency Response of Small Open - Circuited Coaxial Lines Driven With a Source Impedance Equal to their Nominal Characteristic Impedance

As discussed in the previous section, we are up to the point in the frequency domain calculation where we have the values for the complex propagation constant, γ , and complex characteristics impedance, Z_o, versus frequency. Referring to the circuit of Fig. 1, this allows us to , given $V_{in}(f)$ and Z_{in}, use Eqs. 32 (or 33) to get Z_1 given the load impedance Z_2, Eq. 34 to get V_1, and Eq. 35 to get the load voltage, V_2. Here we will take the case of the Z_o (nominal) = 50.00Ω impedance copper coax lines, with a source resistance of R_{in} = 50.00Ω ($Z_{in} = 50.00\Omega + j\,0.0\Omega$). We will take the case of an open-circuited line (a CMOS-like matched source, open load configuration), $Z_2 = \infty$, so that we use Eq. 33 to get Z_1. We take an input signal of V_{in} = 1.0 + j 0.0 volts at all frequencies, in order that the magnitude of $V_2(f)$ will represent the line response directly. Fig. 23 shows the magnitude of $V_2(f)$ versus frequency from 10MHz to 7GHz for an l = 12" length (t_{pd} = 2ns) of 1 mil center conductor diameter copper coax, ε_r = 3.90, source terminated with open load. This case corresponds to an end to end dc resistance of about $R_{dc}\,l$ = 12.2Ω, which would be judged adequate for digital interconnects. The magnitude of $V_2(f)$ increases from 1.0000V at f = 0 (dc), to 1.00011V at 20MHz, holding at 0.9987V at 40MHz before dropping to $|V_2(f)|$ = 0.95V at 100MHz. This unexpected rise (from a nominally source terminated line, which should give a smooth fall) is part of an oscillatory fluctuation on the response characteristic, as seen in Fig. 23. The first dip in this response is at f = 225MHz, the second peak at about 300MHz, the second dip about

470MHz, etc. The 3dB bandwidth is about 860MHz, and the 6dB bandwidth is about 3.337 GHz.

Fig. 24 shows the same $V_2(f)$ versus f curve for a 12" length of 1/2 mil diameter center conductor coax. Reducing the coaxial line conductor dimensions by 2x essentially quadruples the loss in the low frequency region, (the end to end line resistance, R_{dc} $l = 48.8\Omega$ in this case), and should double the loss at high frequencies. Here, $|V_2(f)|$ = 0.995at 10MHz, 0.98 at 20MHz, 0.959 at 30MHz and is 0.90 at 50MHz, falling to 0.75 at 100MHz. The 3 dB bandwidth is about 120MHz and the 6 dB bandwidth about 775MHz. In spite of the steep falloff of $|V_2(f)|$ for the 1/2 mil coax case, the ripple noted for the 1 mil case in Fig. 23 is clearly visible in Fig. 24.

The reason for this ripple in the frequency response characteristics is the fact that the actual complex line impedances, Z_o, as seen in Figs. 21 and 22 for these two cases, are substantially above the nominal 50.00Ω impedance to which R_{in} was matched. For example, an $R_{dc} = 0$, skin effect only calculation using Eqs. 9 and 10 instead of Eqs. 40 and 41 enhances the ripple ($|V_2|$ going to about 1.022 at 61MHz, for example), as seen in Fig. 25. Since this $R_{dc} = 0$ case seriously overestimates L_{int} at low frequencies, the corresponding Z_o values should be too high as well. On the other hand, when the value of Z_o is artificially forced to $Z_o = 50.00 + j\,0.0\Omega$ in the calculation, instead of using Eq. 28, the resulting $|V_2(f)|$ vs. f curve (see Fig. 26) falls monotonically, with no noticeable sign of ripple as in Figs. 23 and 24. It can be concluded from this that the variations of Z_o with f can have significant effects on real MCM interconnect signal quality.

1.6. Application of Numerical Inverse Fourier Transform To Obtain Time Domain Waveforms

In the general case of the application of Fourier transform techniques to obtaining time domain signal waveforms, FFT/iFFT pairing is used to obtain the convolution of the input signal waveform with the line response. The input waveform is transformed into the frequency domain where it becomes the V_{in} generator in Fig. 1. Since the output of the transmission line calculation, V_2, is proportional to V_{in} (and correspondingly tracks its phase), this amounts to multiplication in the frequency domain, which is precisely how time domain convolution is accomplished using the FFT/iFFT operation. Hence, the iFFT of $V_2(f)$ back into the time domain represents the convolution of the input waveform with the impulse response function of the linear system (transmission line circuit). While we may be utilizing this software for this purpose later, at this point most of the effort has been on obtaining the impulse response of the lossy transmission line circuit using the iFFT, and then doing a simple trapezoidal rule integration of the impulse response result to get the step response.

One advantage of using a transformed waveform for V_{in} is that the finite risetime of the waveform will tend to reduce the amplitude of the high frequency components in $V_2(f)$. This would be helpful, since if the transmission line segment is not lossy enough, it may not be practical to do enough points in the iFFT array to keep aliasing of high frequency components (beyond the Nyguist limit) from interfering with the accuracy of the calculation. Early on, I successfully used a step function input (just divide the $V_2(f)$ by $j\omega$ to do this) for the calculation. While the $1/j\omega$ factor helps reduce the high frequency spillover, it blows up at zero frequency and the error due to finite frequency step size at the low frequency end (between dc and the first ac point), leads to both a dc offset and a major slope error which must be corrected out to give useful results. Hence, I decided to use a simple $V_{in} = (1,0)$ frequency domain input (corresponding to a δ - function at t = 0 time domain input), which makes $V_2(t)$, the iFFT of $V_2(f)$, the impulse response of the system. If everything is done correctly, the iFFT of the complex $V_2(f)$ waveform should have a real part (the time domain impulse response waveform), but no imaginary

part. This was the case for the analysis here. To insure that the time step-frequency step conversions and the iFFT waveform normalization, a standard Fourier transform pair (critically damped exponential pulse) was evaluated and found to give very accurate results. The simple 2-point trapezoidal rule integration was selected over 3-point Simpson's rule because of its even weighing of all points in the integral. Since there tends to be some "ping - ponging" (alternate + and - errors) in the iFFT impulse response due to feedthru which tends to average out, it is important that the integral method give an even weighing to all points. The results with the simple trapezoidal rule integration seem fine, with step heights generally very precisely 1.0000.

The case of the l = 12 inches long 1 mil center conductor coax calculation is shown in Figs. 27 - 29. Fig. 27 shows the magnitude of $V_2(f)$ versus f at a frequency of 61.0351562$5$MHz / point over the frequency range of f = 0 to 25GHz. This magnitude data is extracted from the complex $V_2(f)$ array from which the iFFT is taken. It is necessary to go to such high frequencies in order to insure that the magnitude of $V_2(f)$ is adequately small above this upper frequency limit. The results of this 8192 point iFFT, $V_2(t)$, is shown as the impulse response in Fig. 29 (the real part is shown, the imaginary part is zero). This may be interpreted as a voltage slew rate (dV/dt). The peak value in Fig. 29 is a slew rate of about 20.5 volts / nanosecond. The arrival time is correct for an l = 0.3048 meter line with ε_r = 3.90. Figure 29 shows the step response, V2int obtained by integrating the real part of the iFFT result, $V_2(t)$. The waveform, with no correction of any kind (for offset or slope gives the proper zero response before t_{pd} ~2ns, a reasonable looking rise, and an ultimate value of 1.0000V. It does have a slight overshoot "hump" at t = 6ns (2 t_{pd} past arrival), going to a peak amplitude of 1.021845V at 6.084ns. The rise curve is 0.3% at 2.01ns, 2.2% at 2.012ns, 9.8% at 2.016ns, 20.75% at 2.022ns, 40.13% at 2.040ns, 50.1% at 2.058ns, 59.92% at 2.086ns, 69.95% at 2.158ns, 79.98% at 2.332ns, 85% at 2.53ns, 90% at 2.910ns, and 95% at 3.647ns. Past the "hump", the step amplitude drops to 0.999940298V at 13.322ns, ending at 0.999999981V at 16.328ns in the 8192 point array (2.0 ps/step). The "hump" response is real, the result of the frequency dependent Z_o, corresponding to the "ripple" seen in $V_2(f)$. In

the case of the $R_{dc} = 0$, skin effect only analysis shown in Figs. 30 and 31 for the same $l = 12$" 1 mil center conductor diameter coax, the result is a more pronounced "hump" with nearly 4% overshoot, corresponding to the higher ripple in $V_2(f)$ seen in Fig. 25 for this $R_{dc} = 0$ case. On the other hand, as shown in Fig. 32 for the case where Z_o was forced to be $Z_o = 50.00\Omega + j\,0.0\Omega$(as shown in Fig. 26), there is no hump and a remarkably erfc-like behavior (as suggested by Eqs. 14-18) is observed. This would appear to point to the "hump" as being a real consequence of the frequency dependence of Z_o in these small lines, and not some calculational artifact.

Figures 33-35 show the case for the 1/2 mil diameter center conductor coax, also $l =$ 12 inches long. Because of the higher alternation in the smaller center conductor, little signal output is seen beyond 10GHz in Fig. 33. Correspondingly, the maximum voltage slew rate in Fig. 34 is smaller, less than 5 volts/ns. The step response for this $R_{dc}\,l = 48.8\Omega$ case shows the same kind of pronounced R_{dc} sloping segment effects discussed at length in last month's report, and seen, for example in Fig. 12.

In summary, the results of this full-blown frequency domain / iFFT interconnect line simulation appears to be physically meaningful and offer important insights into line behavior.

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6. SBIR Final Report, "High Density Multi-Layer Interconnects for High Speed Digital MCMs", DARPA BAA 90-114, Contract DAAG01-91-C-R038, December 1991.

7. "Reference Data for Engineers: Radio, Electronics, Computer and Communications - Seventh Edition", Edward C. Jordan, SAMS, Carmel, Indiana, ISBN 0-672-21563-2, Chapter 29, pp. 29-1 to 29-7.

8. Abramowite and Stegun, "Handbook of Mathematical Functions", National Bureau of Standards Applied Mathematics Series 55, US Government Printing Office, Wash. DC, Sections 9.9 - 9.11 and Table 9.12.

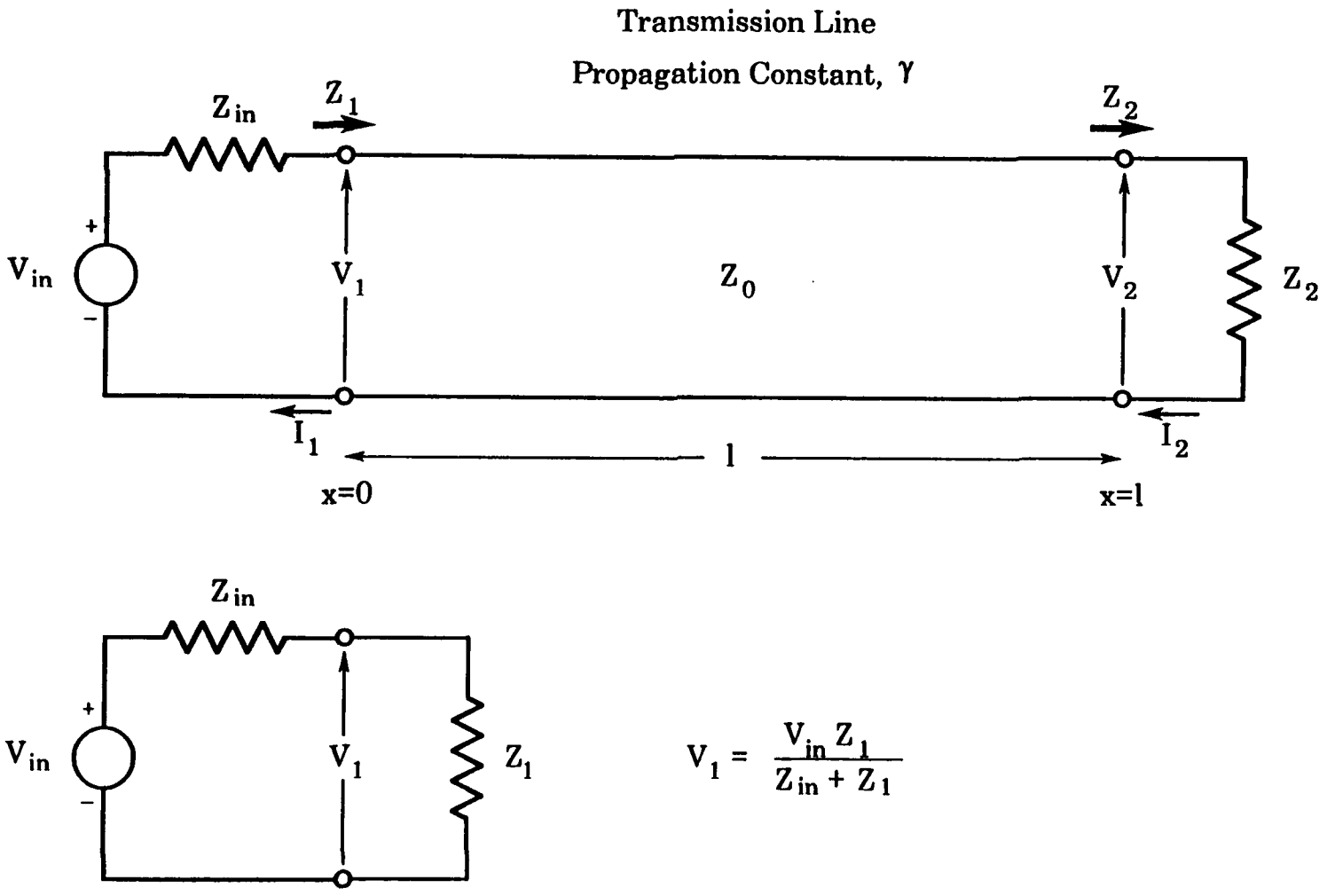
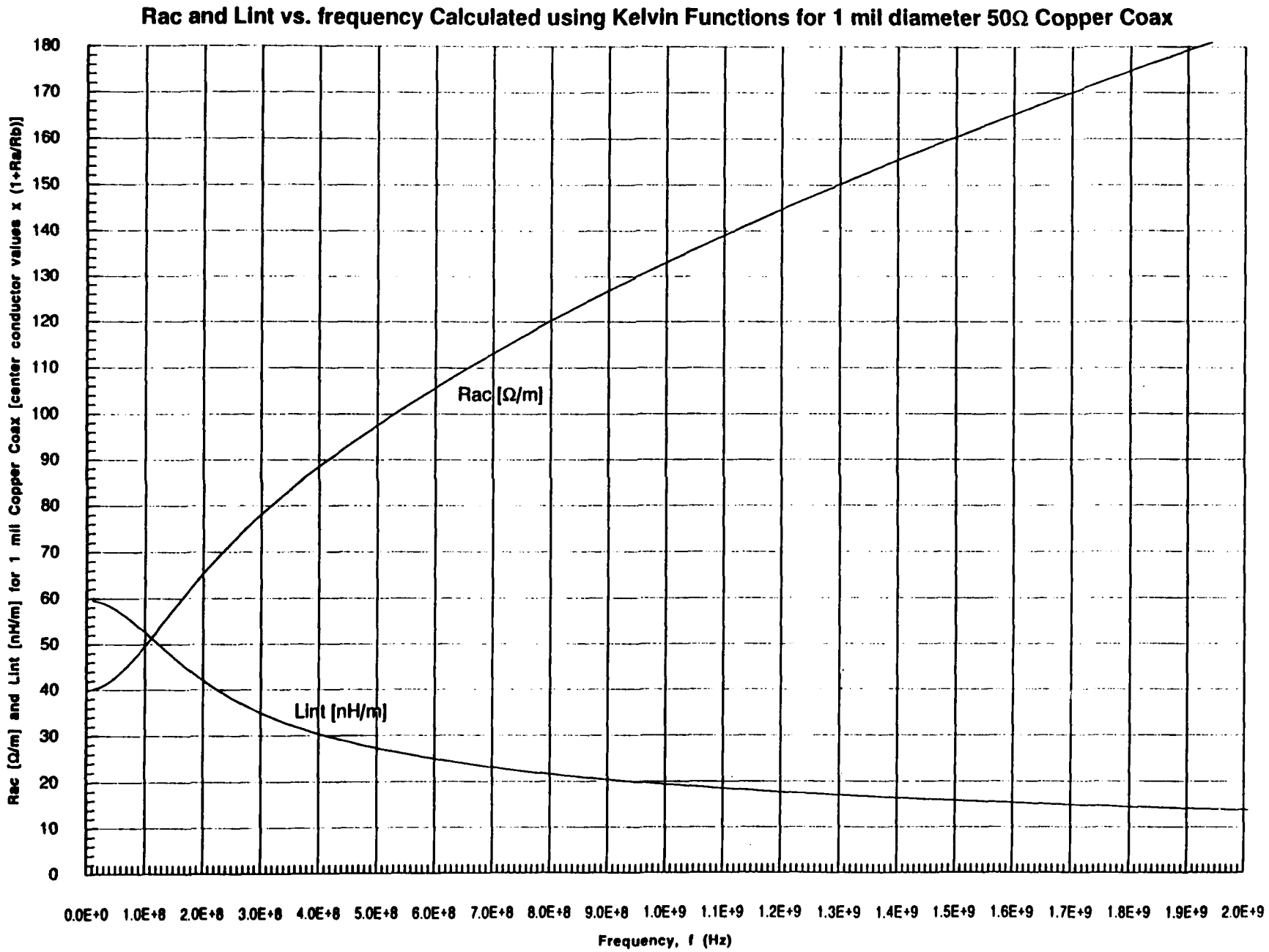

Transmission Line
Propagation Constant, γ
Z in
Z 1
Z 2
V in
V 1
Z 0
V 2
Z 2
I 1
I 2
l
x=0
x=l
Z in
V in
V 1
Z 1
V 1 = V in Z 1 / (Z in + Z 1)

Figure 16


Rac and Lint vs. frequency Calculated using Kelvin Functions for 1 mil diameter 50Ω Copper Coax
Rac [Ω/m] and Lint [nH/m] for 1 mil Copper Coax [center conductor values x (1+Ra/Rb)]
180
170
160
150
140
130
120
110
100
90
80
70
60
50
40
30
20
10
0
Rac [Ω/m]
Lint [nH/m]
0.0E+0 1.0E+8 2.0E+8 3.0E+8 4.0E+8 5.0E+8 6.0E+8 7.0E+8 8.0E+8 9.0E+8 1.0E+9 1.1E+9 1.2E+9 1.3E+9 1.4E+9 1.5E+9 1.6E+9 1.7E+9 1.8E+9 1.9E+9 2.0E+9
Frequency, f (Hz)

Equation 17

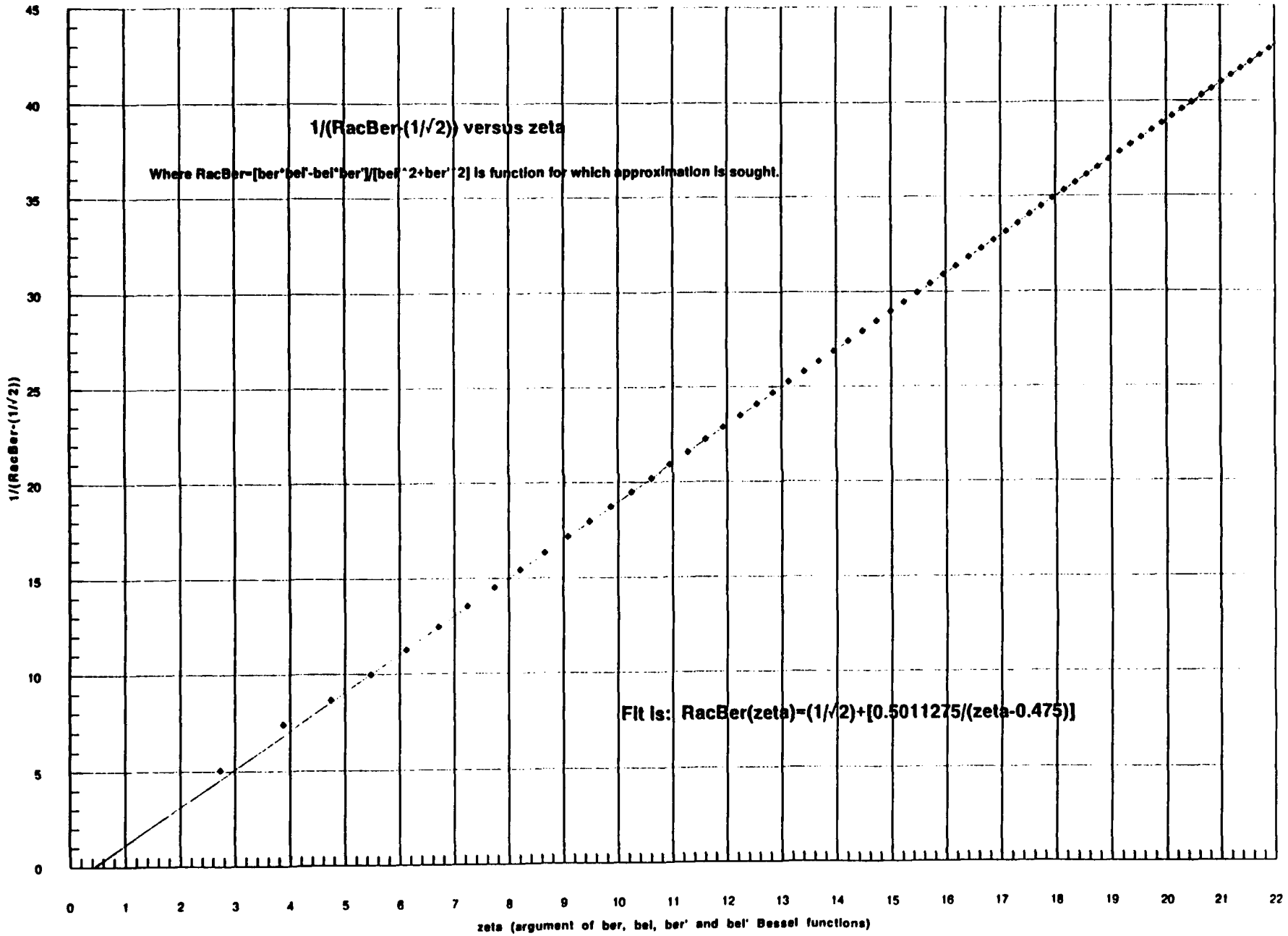

1/(RacBer-(1/√2)) versus zeta
Where RacBer=[ber*bei'-bei*ber']/[bei^2+ber'^2] is function for which approximation is sought.
Fit is: RacBer(zeta)=(1/√2)+[0.5011275/(zeta-0.475)]
1/(RacBer-(1/√2))
zeta (argument of ber, bei, ber' and bei' Bessel functions)
0
5
10
15
20
25
30
35
40
45
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22

Figure 18

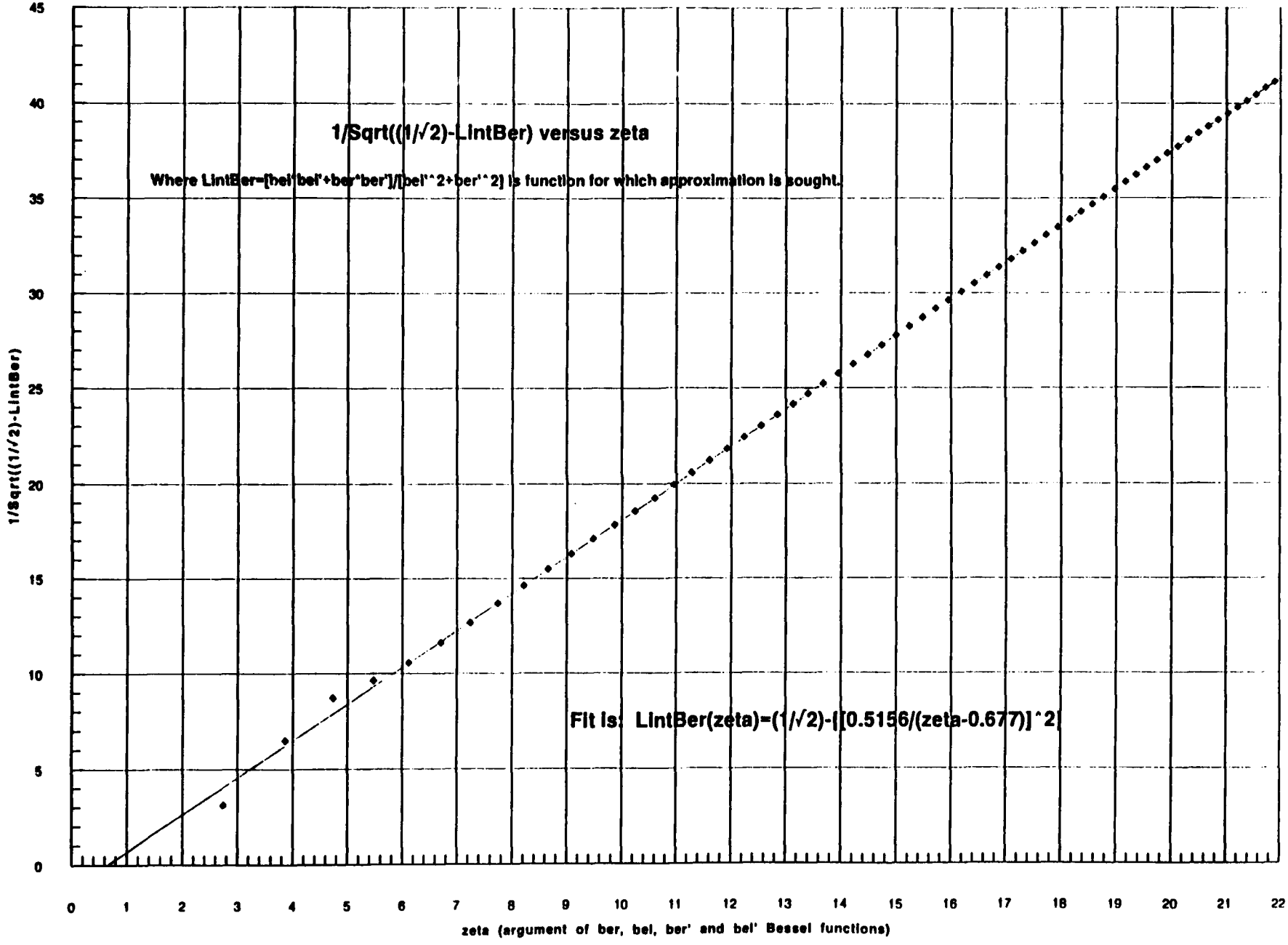

1/Sqrt((1/√2)-LintBer) versus zeta
Where LintBer=[bei'bei'+ber'ber']/[bei'^2+ber'^2] is function for which approximation is sought.
Fit is: LintBer(zeta)=(1/√2)-[[0.5156/(zeta-0.677)]^2
1/Sqrt((1/√2)-LintBer)
zeta (argument of ber, bei, ber' and bei' Bessel functions)
0
5
10
15
20
25
30
35
40
45
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22

Figure 19

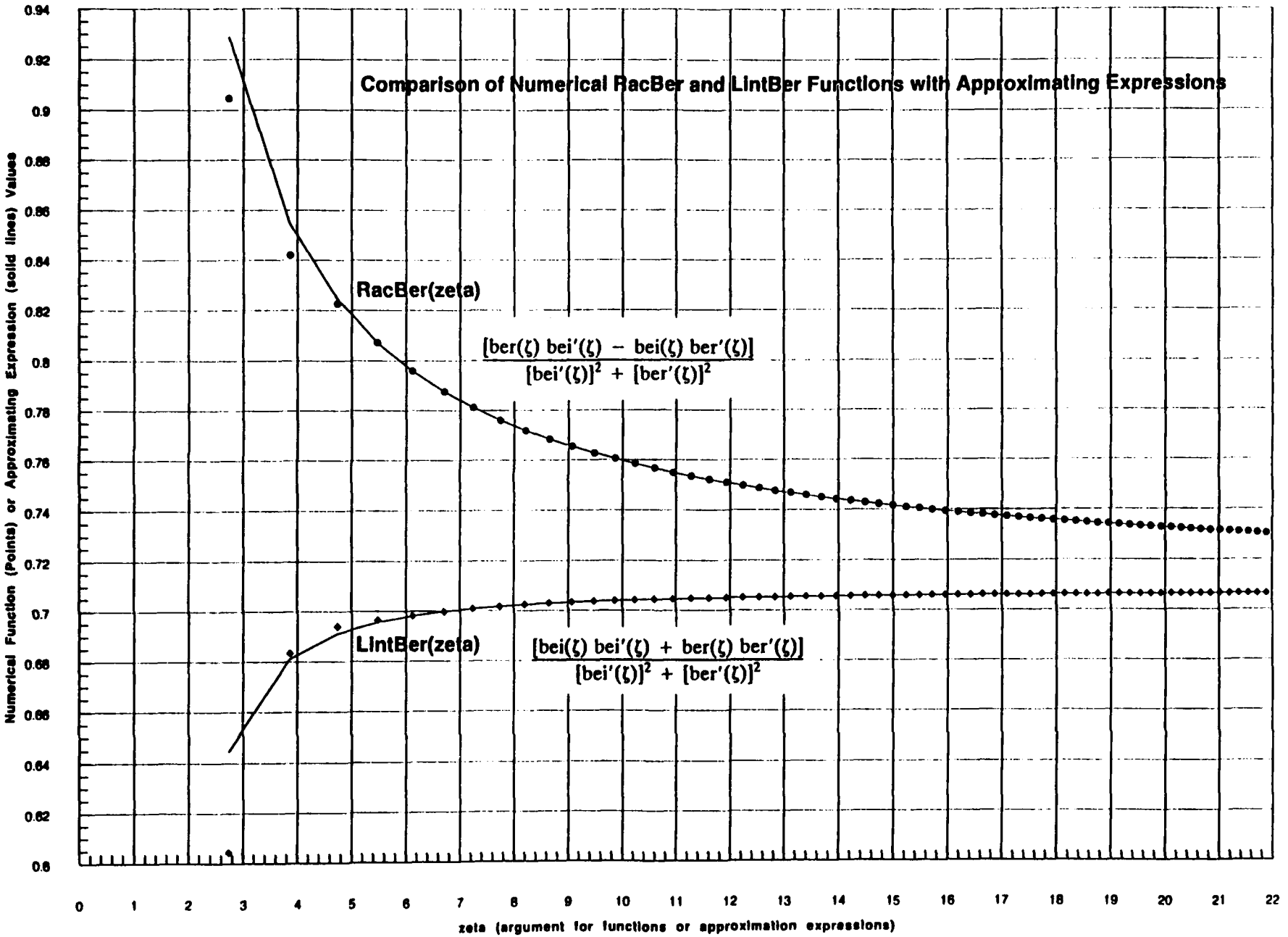

Comparison of Numerical RacBer and LintBer Functions with Approximating Expressions
RacBer(zeta)
[ber(ζ) bei'(ζ) − bei(ζ) ber'(ζ)] / [bei'(ζ)]² + [ber'(ζ)]²
LintBer(zeta)
[bei(ζ) bei'(ζ) + ber(ζ) ber'(ζ)] / [bei'(ζ)]² + [ber'(ζ)]²
Numerical Function (Points) or Approximating Expression (solid lines) Values
0.94
0.92
0.9
0.88
0.86
0.84
0.82
0.8
0.78
0.76
0.74
0.72
0.7
0.68
0.66
0.64
0.62
0.6
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
zeta (argument for functions or approximation expressions)

Figure 20

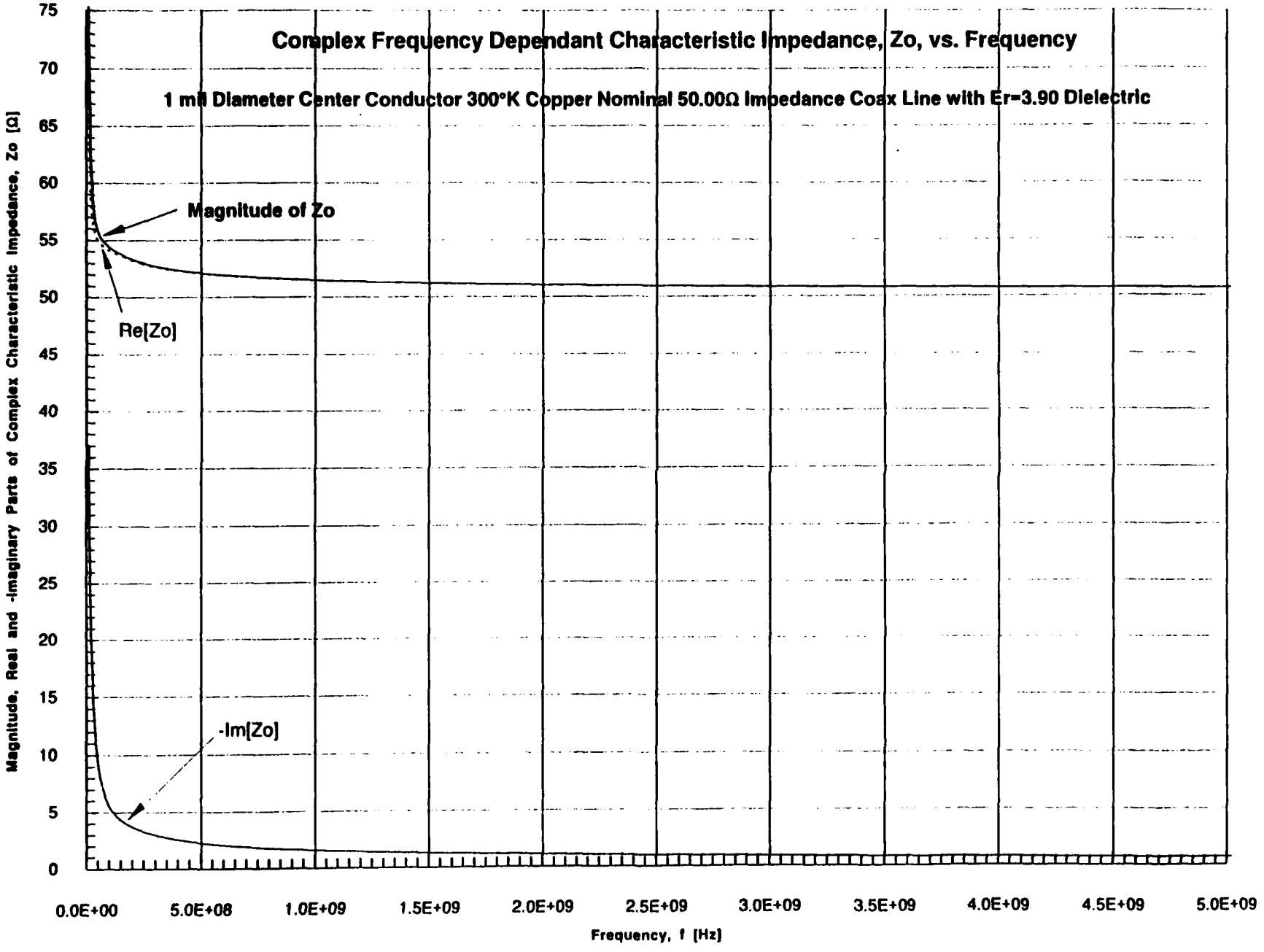

Complex Frequency Dependant Characteristic Impedance, Zo, vs. Frequency
1 mil Diameter Center Conductor 300°K Copper Nominal 50.00Ω Impedance Coax Line with Er=3.90 Dielectric
Magnitude of Zo
Re[Zo]
-Im[Zo]
Magnitude, Real and -Imaginary Parts of Complex Characteristic Impedance, Zo [Ω]
75
70
65
60
55
50
45
40
35
30
25
20
15
10
5
0
0.0E+00
5.0E+08
1.0E+09
1.5E+09
2.0E+09
2.5E+09
3.0E+09
3.5E+09
4.0E+09
4.5E+09
5.0E+09
Frequency, f [Hz]

Figure 21

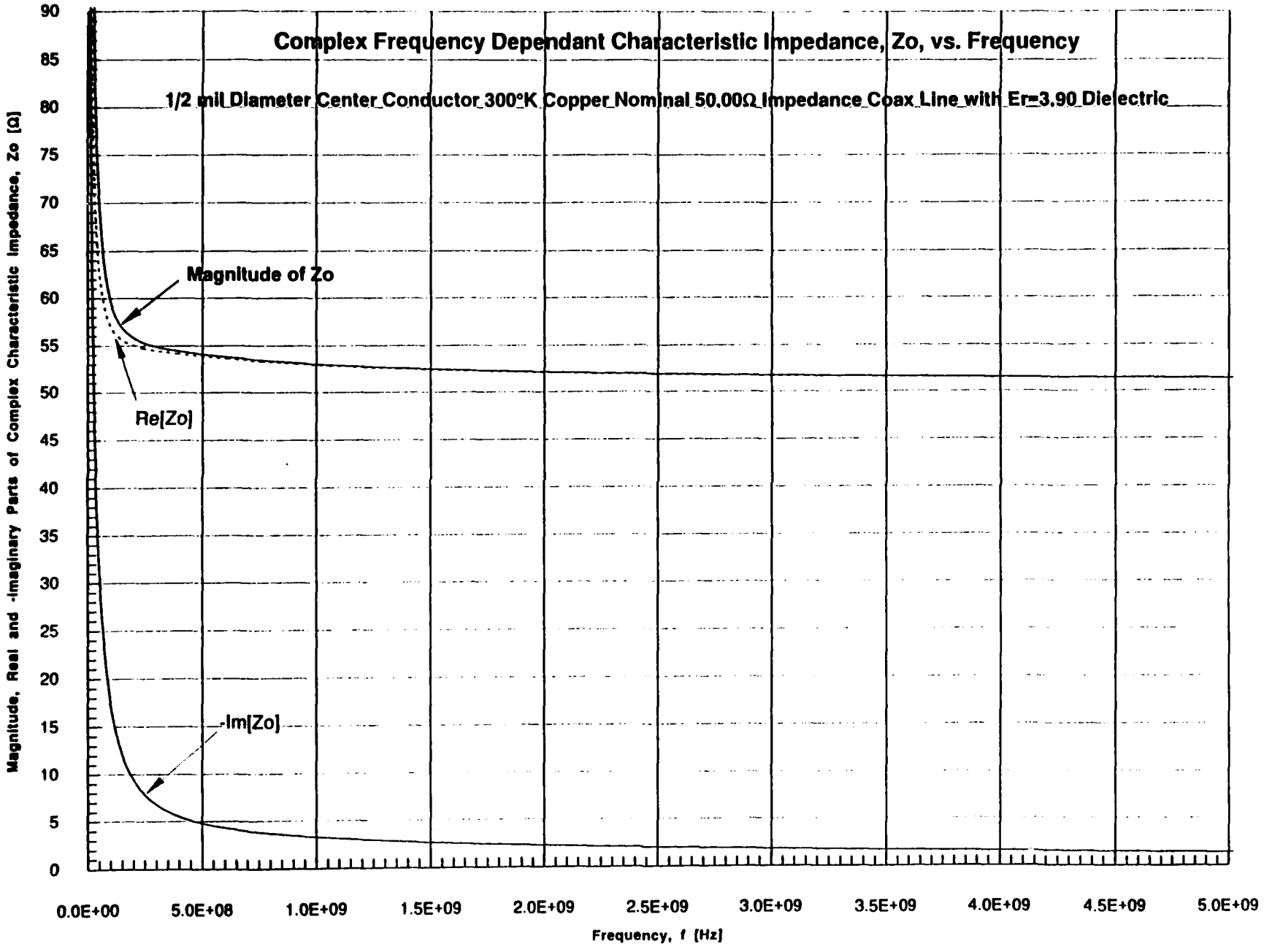

Complex Frequency Dependant Characteristic Impedance, Zo, vs. Frequency
1/2 mil Diameter Center Conductor 300°K Copper Nominal 50.00Ω Impedance Coax Line with Er=3.90 Dielectric
Magnitude of Zo
Re[Zo]
Im[Zo]
Magnitude, Real and -Imaginary Parts of Complex Characteristic Impedance, Zo [Ω]
Frequency, f [Hz]
0
5
10
15
20
25
30
35
40
45
50
55
60
65
70
75
80
85
90
0.0E+00
5.0E+08
1.0E+09
1.5E+09
2.0E+09
2.5E+09
3.0E+09
3.5E+09
4.0E+09
4.5E+09
5.0E+09

Figure 22

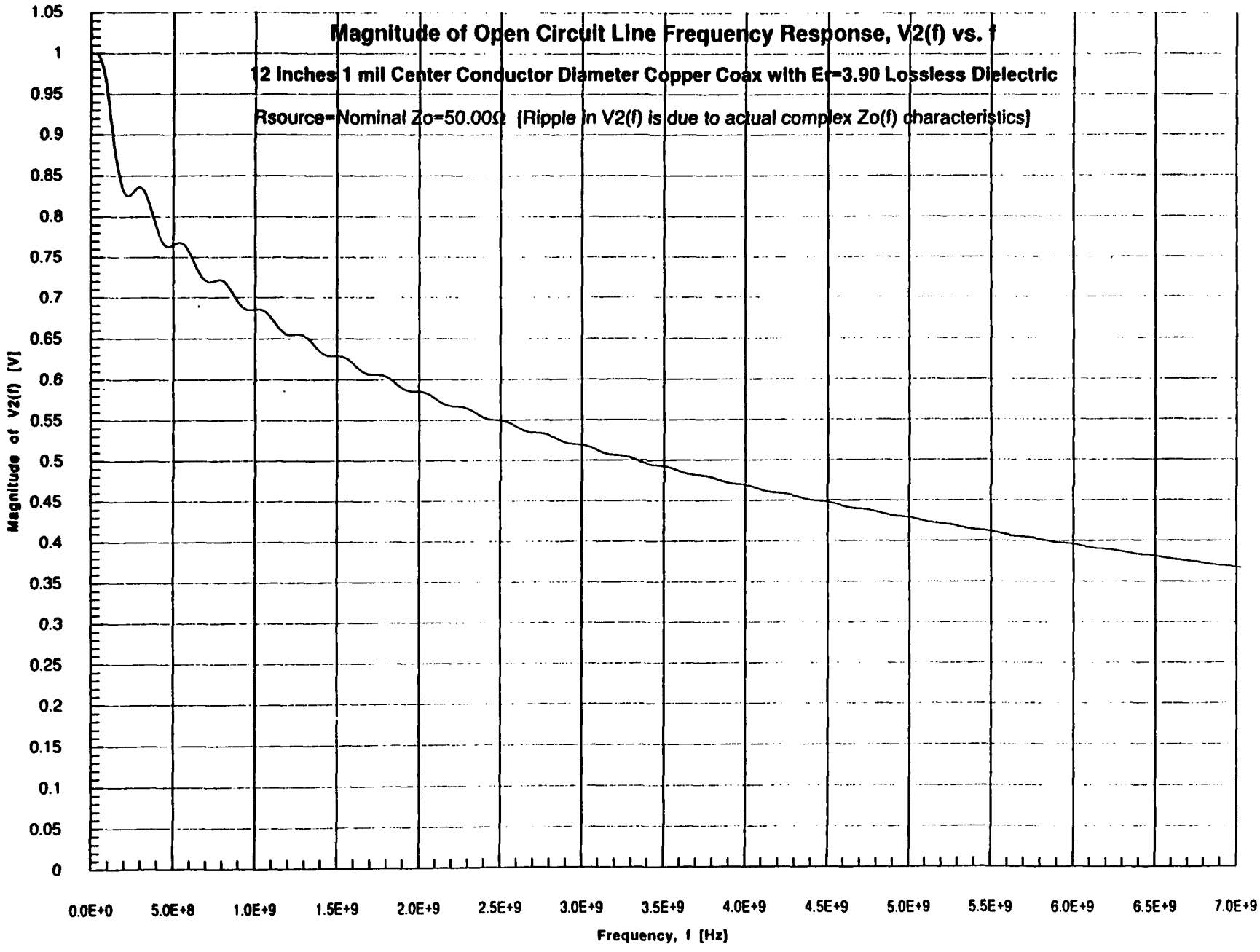

Magnitude of Open Circuit Line Frequency Response, V2(f) vs. f
12 inches 1 mil Center Conductor Diameter Copper Coax with Er=3.90 Lossless Dielectric
Rsource=Nominal Zo=50.00Ω [Ripple in V2(f) is due to actual complex Zo(f) characteristics]
Magnitude of V2(f) [V]
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0.0E+0
5.0E+8
1.0E+9
1.5E+9
2.0E+9
2.5E+9
3.0E+9
3.5E+9
4.0E+9
4.5E+9
5.0E+9
5.5E+9
6.0E+9
6.5E+9
7.0E+9
Frequency, f [Hz]

Figure 23

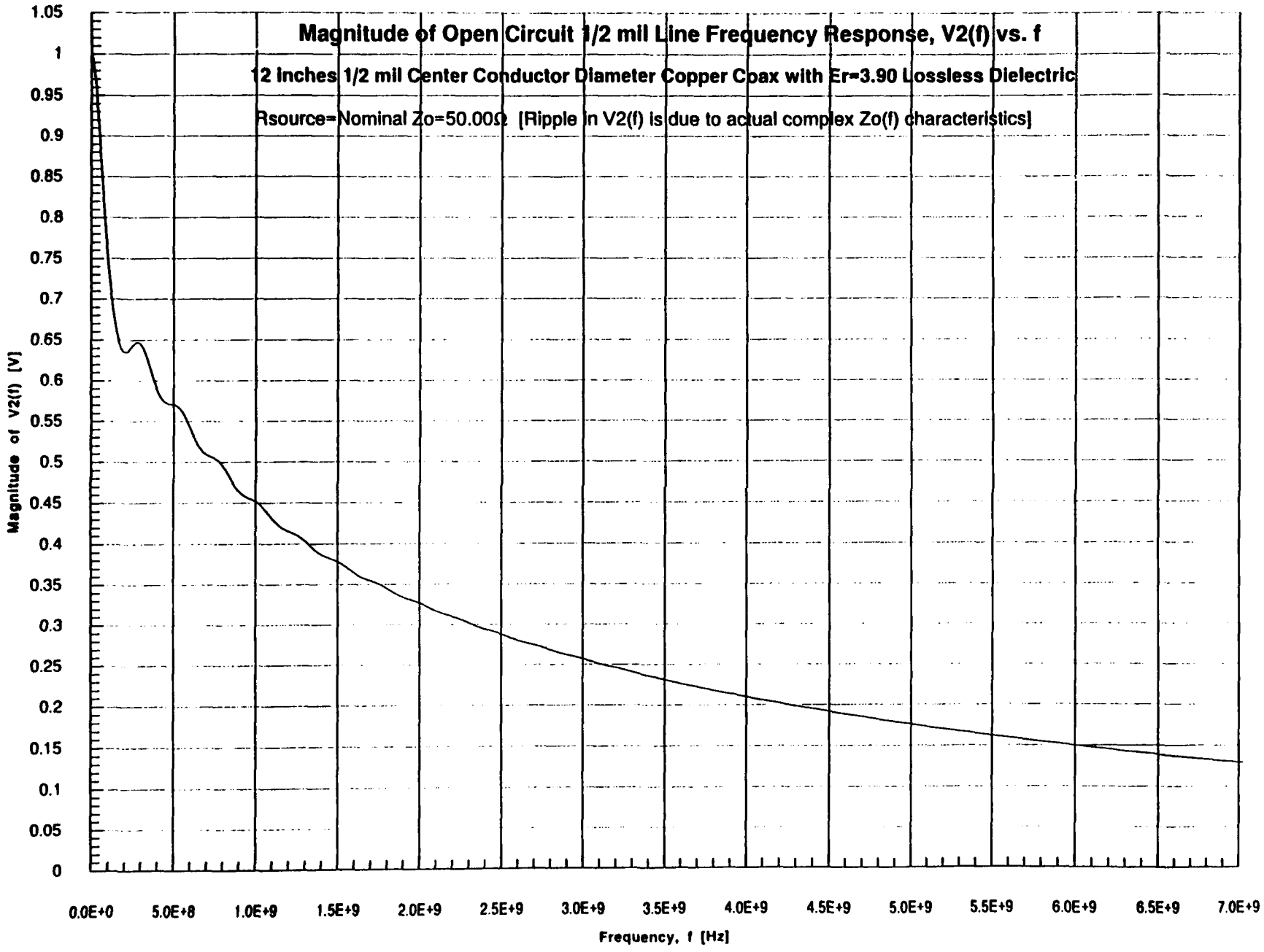

Magnitude of Open Circuit 1/2 mil Line Frequency Response, V2(f) vs. f
12 Inches 1/2 mil Center Conductor Diameter Copper Coax with Er=3.90 Lossless Dielectric
Rsource=Nominal Zo=50.00Ω [Ripple in V2(f) is due to actual complex Zo(f) characteristics]
Magnitude of V2(f) [V]
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0.0E+0
5.0E+8
1.0E+9
1.5E+9
2.0E+9
2.5E+9
3.0E+9
3.5E+9
4.0E+9
4.5E+9
5.0E+9
5.5E+9
6.0E+9
6.5E+9
7.0E+9
Frequency, f [Hz]

Figure 24

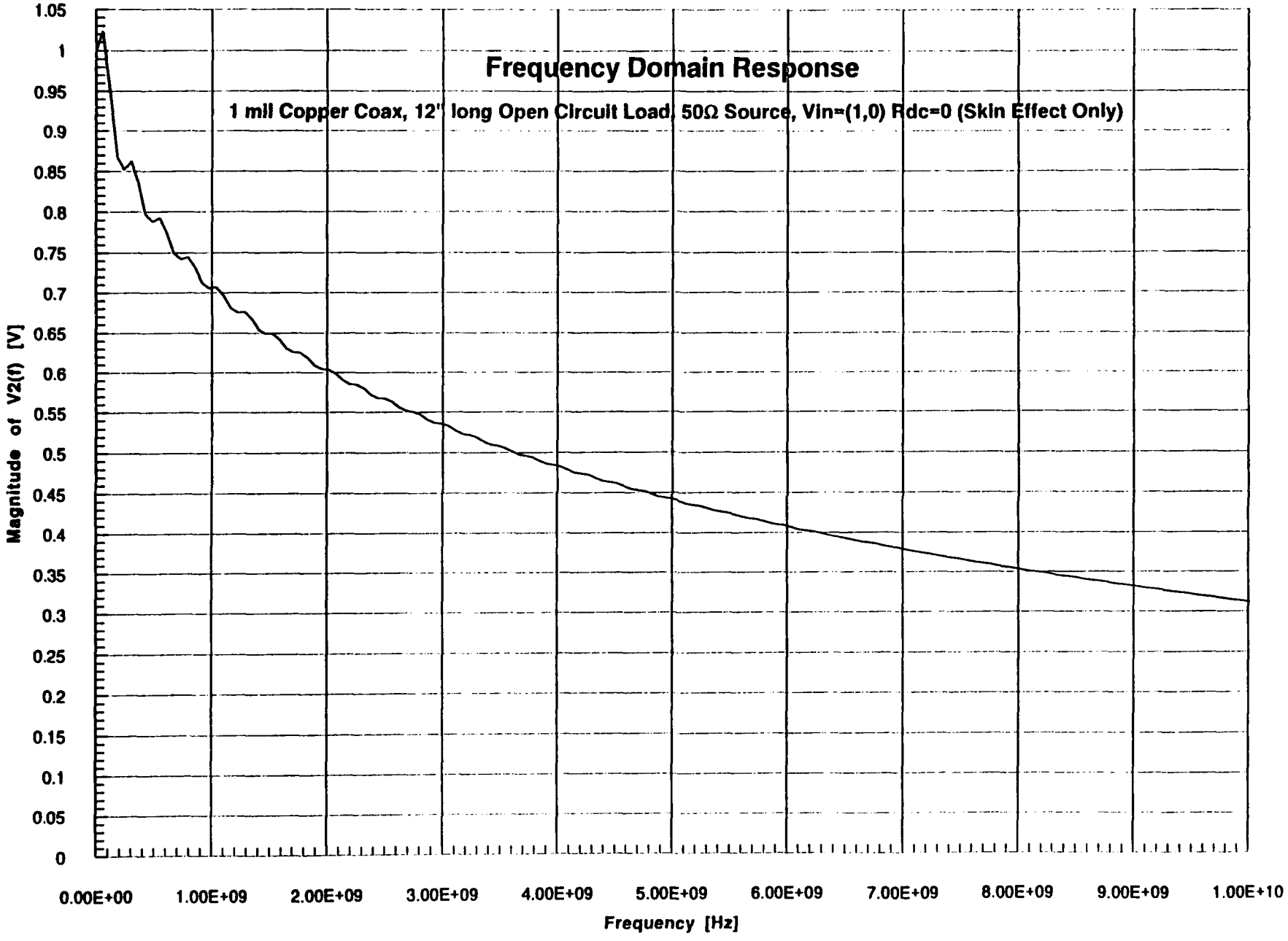

Frequency Domain Response
1 mil Copper Coax, 12" long Open Circuit Load, 50Ω Source, Vin=(1,0) Rdc=0 (Skin Effect Only)
Magnitude of V2(f) [V]
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0.00E+00
1.00E+09
2.00E+09
3.00E+09
4.00E+09
5.00E+09
6.00E+09
7.00E+09
8.00E+09
9.00E+09
1.00E+10
Frequency [Hz]

Figure 25

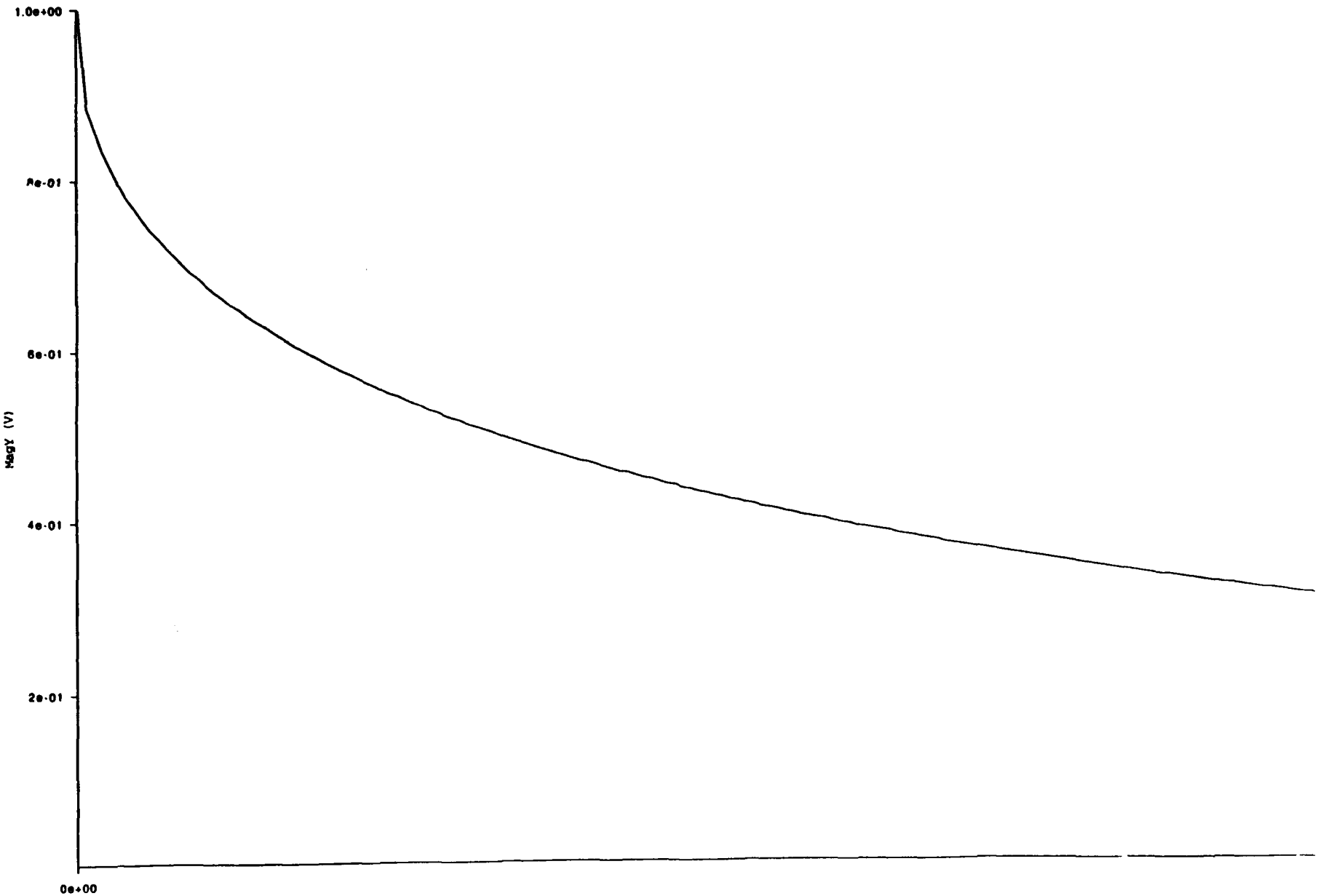

Zo=50.0+j0.0 Ω Frequency Dependence of Magnitude of Open-Circuit Voltage at end of 1 mil Cu Coax Line (Ber/Bel Calc. of Rac and Lint)
1.0e+00
8e-01
6e-01
4e-01
2e-01
0e+00
MagY (V)

Figure 26

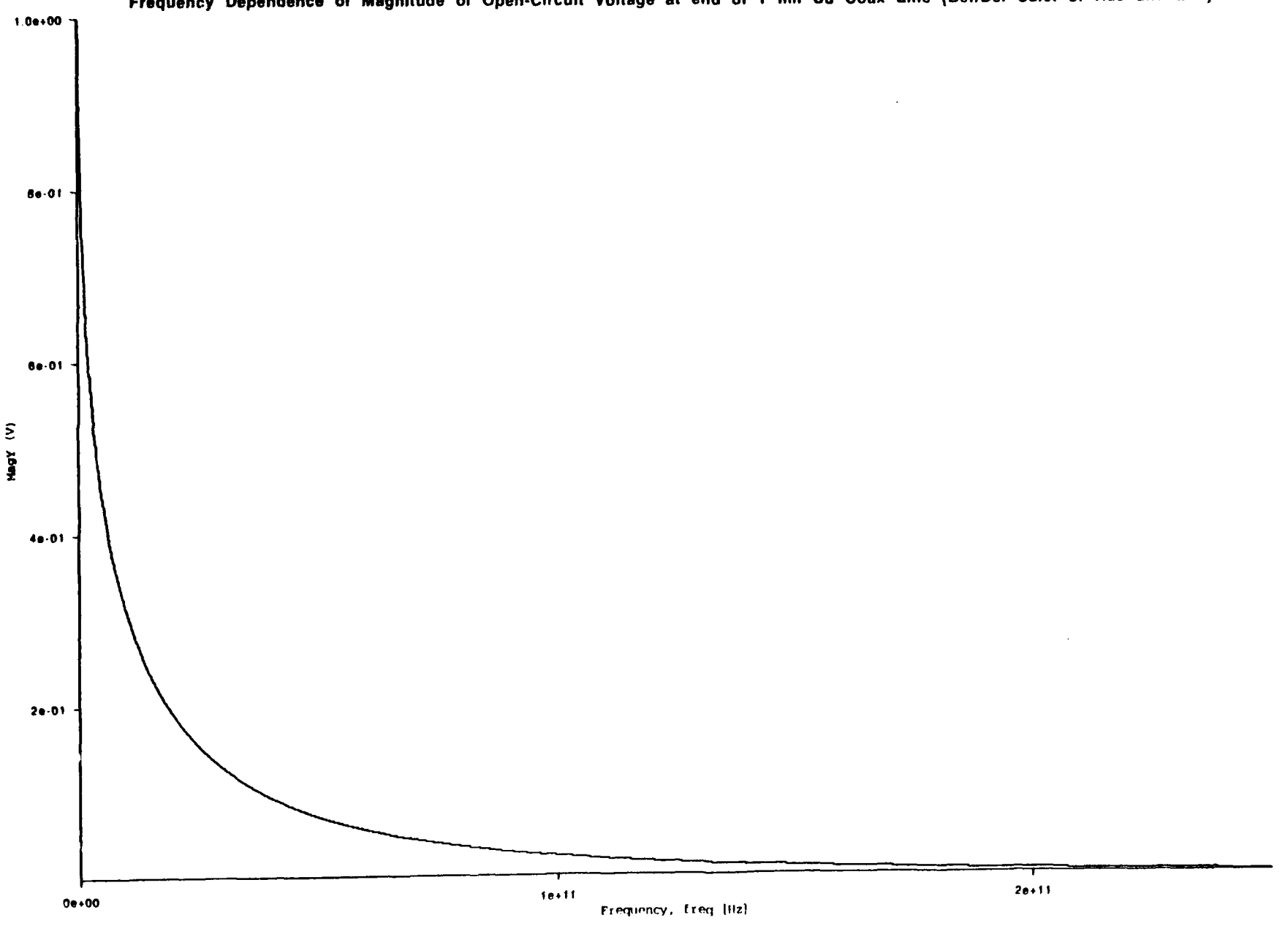

Frequency Dependence of Magnitude of Open-Circuit Voltage at end of 1 mil Cu Coax Line (Ber/Bel Calc. of Rac and Lint)
1.0e+00
8e-01
6e-01
4e-01
2e-01
MagY (V)
0e+00
1e+11
2e+11
Frequency, Freq [Hz]

Figure 27

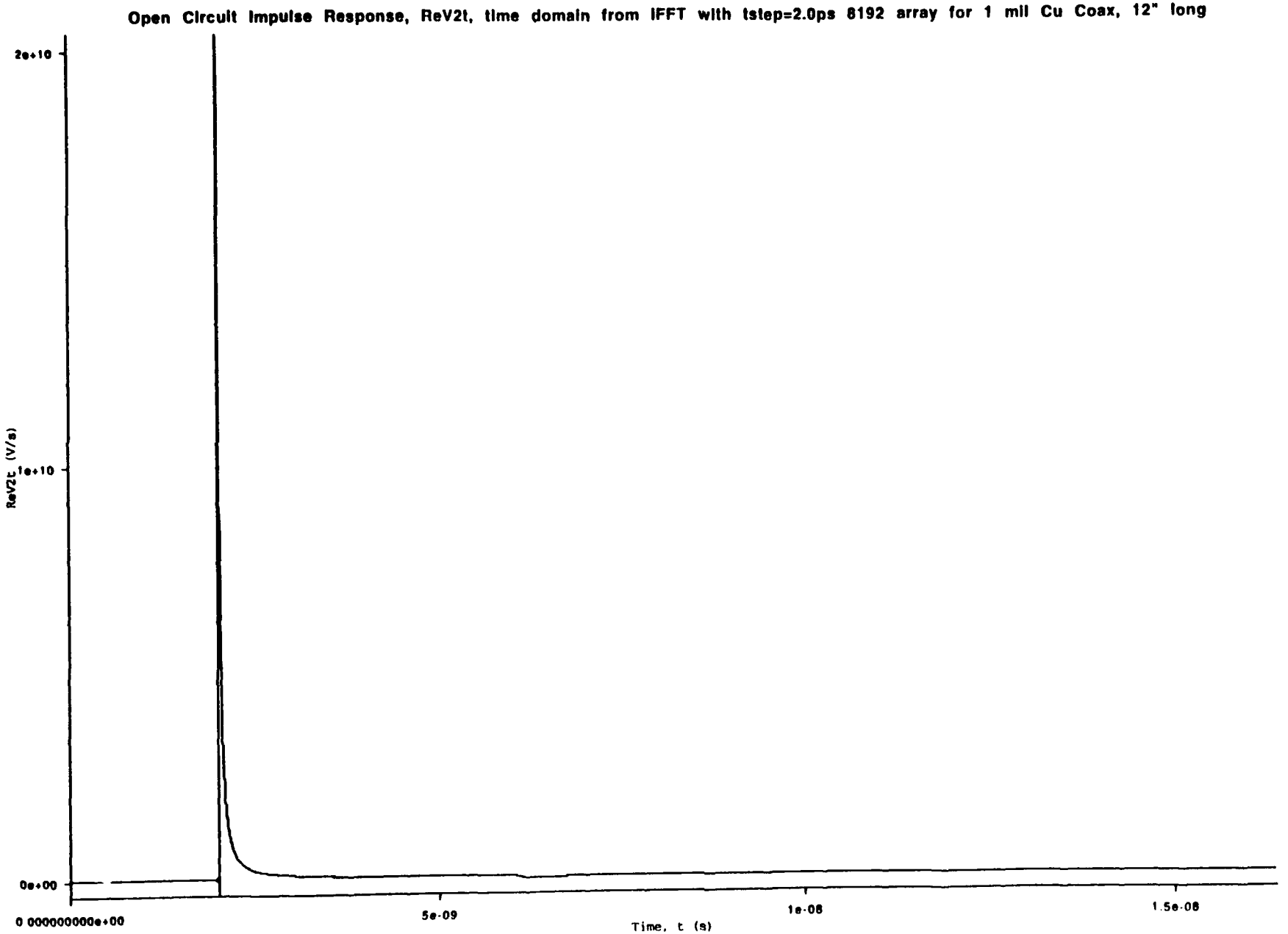

Open Circuit Impulse Response, ReV2t, time domain from IFFT with tstep=2.0ps 8192 array for 1 mil Cu Coax, 12" long
2e+10
1e+10
0e+00
ReV2t (V/s)
0.000000000e+00
5e-09
1e-08
1.5e-08
Time, t (s)

Figure 28

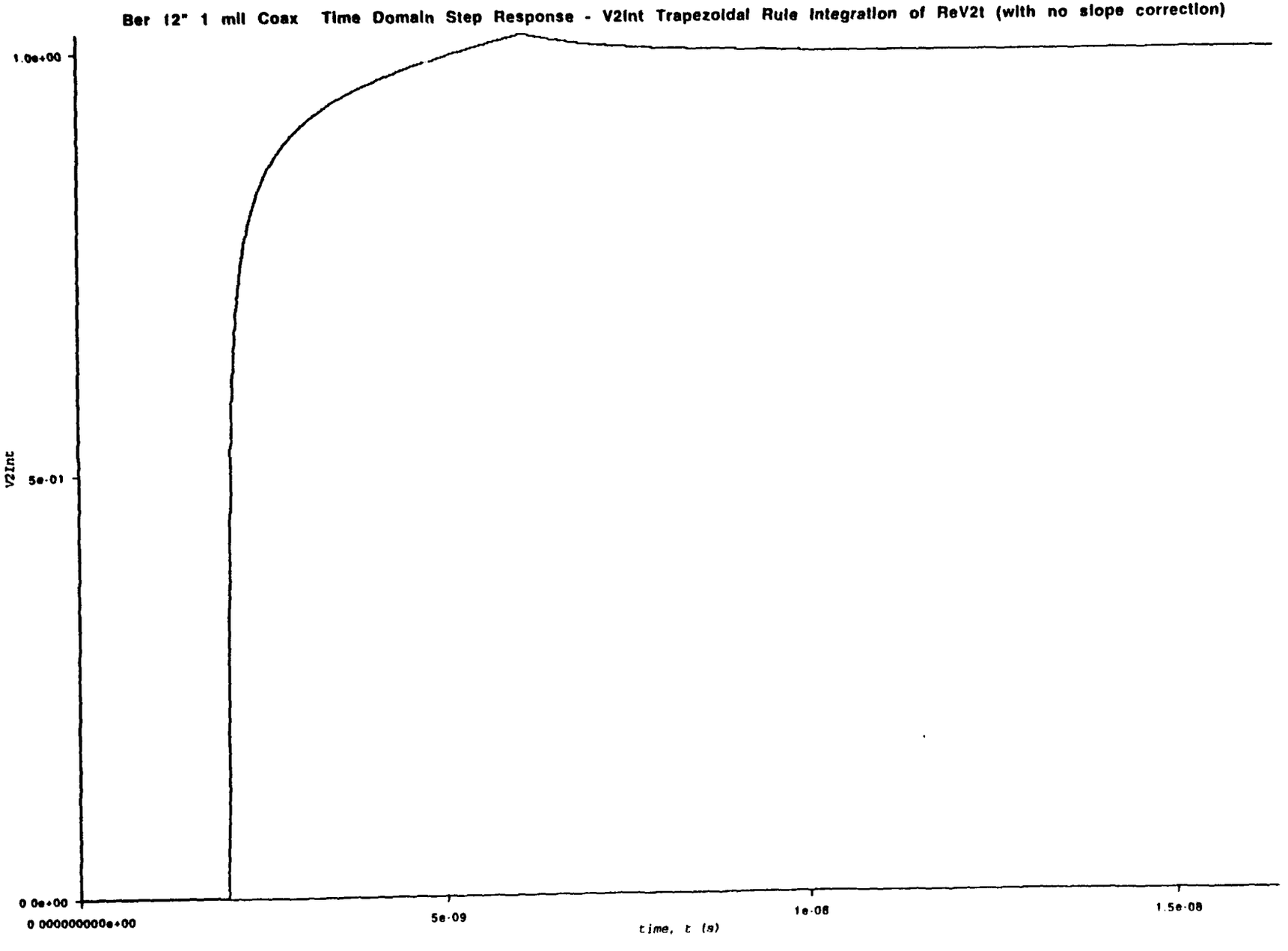

Ber 12" 1 mil Coax Time Domain Step Response - V2int Trapezoidal Rule Integration of ReV2t (with no slope correction)
1.0e+00
5e-01
0.0e+00
V2int
0.000000000e+00
5e-09
1e-08
1.5e-08
time, t (s)

Figure 29

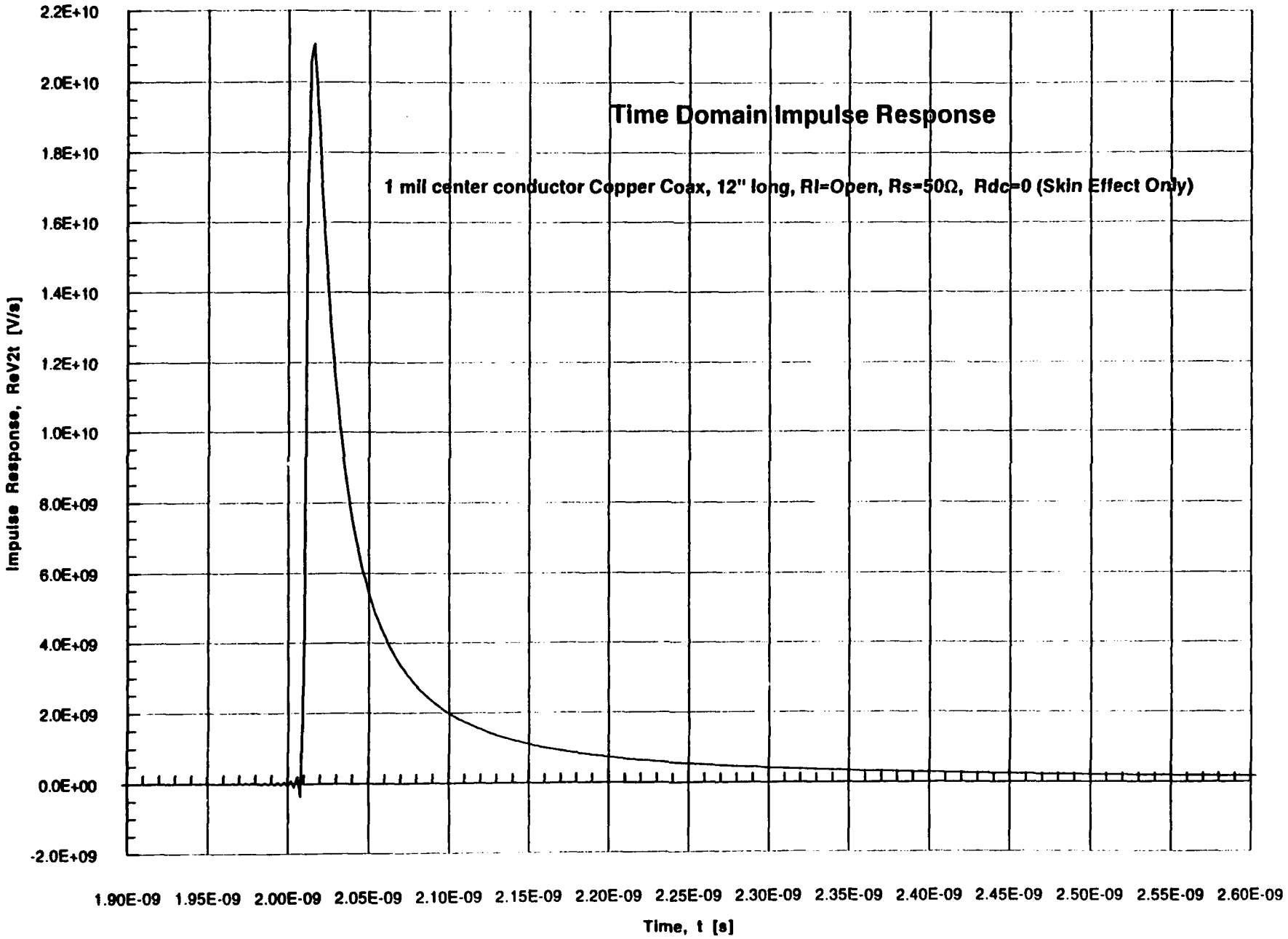

Time Domain Impulse Response
1 mil center conductor Copper Coax, 12" long, Rl=Open, Rs=50Ω, Rdc=0 (Skin Effect Only)
Impulse Response, ReV2t [V/s]
2.2E+10
2.0E+10
1.8E+10
1.6E+10
1.4E+10
1.2E+10
1.0E+10
8.0E+09
6.0E+09
4.0E+09
2.0E+09
0.0E+00
-2.0E+09
1.90E-09 1.95E-09 2.00E-09 2.05E-09 2.10E-09 2.15E-09 2.20E-09 2.25E-09 2.30E-09 2.35E-09 2.40E-09 2.45E-09 2.50E-09 2.55E-09 2.60E-09
Time, t [s]

Figure 30

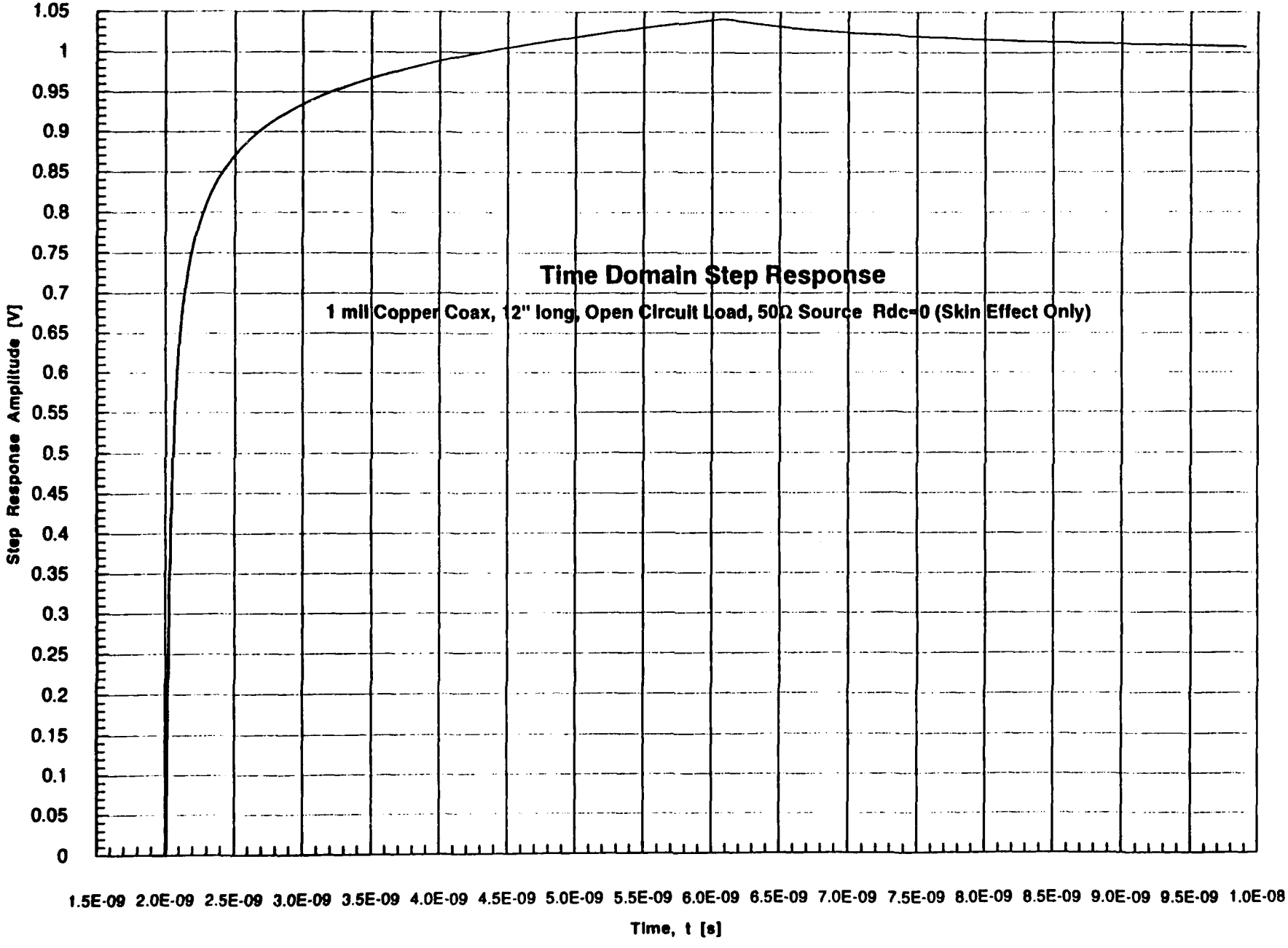

Time Domain Step Response
1 mil Copper Coax, 12" long, Open Circuit Load, 50Ω Source Rdc=0 (Skin Effect Only)
Step Response Amplitude [V]
1.05
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
1.5E-09 2.0E-09 2.5E-09 3.0E-09 3.5E-09 4.0E-09 4.5E-09 5.0E-09 5.5E-09 6.0E-09 6.5E-09 7.0E-09 7.5E-09 8.0E-09 8.5E-09 9.0E-09 9.5E-09 1.0E-08
Time, t [s]

Figure 31

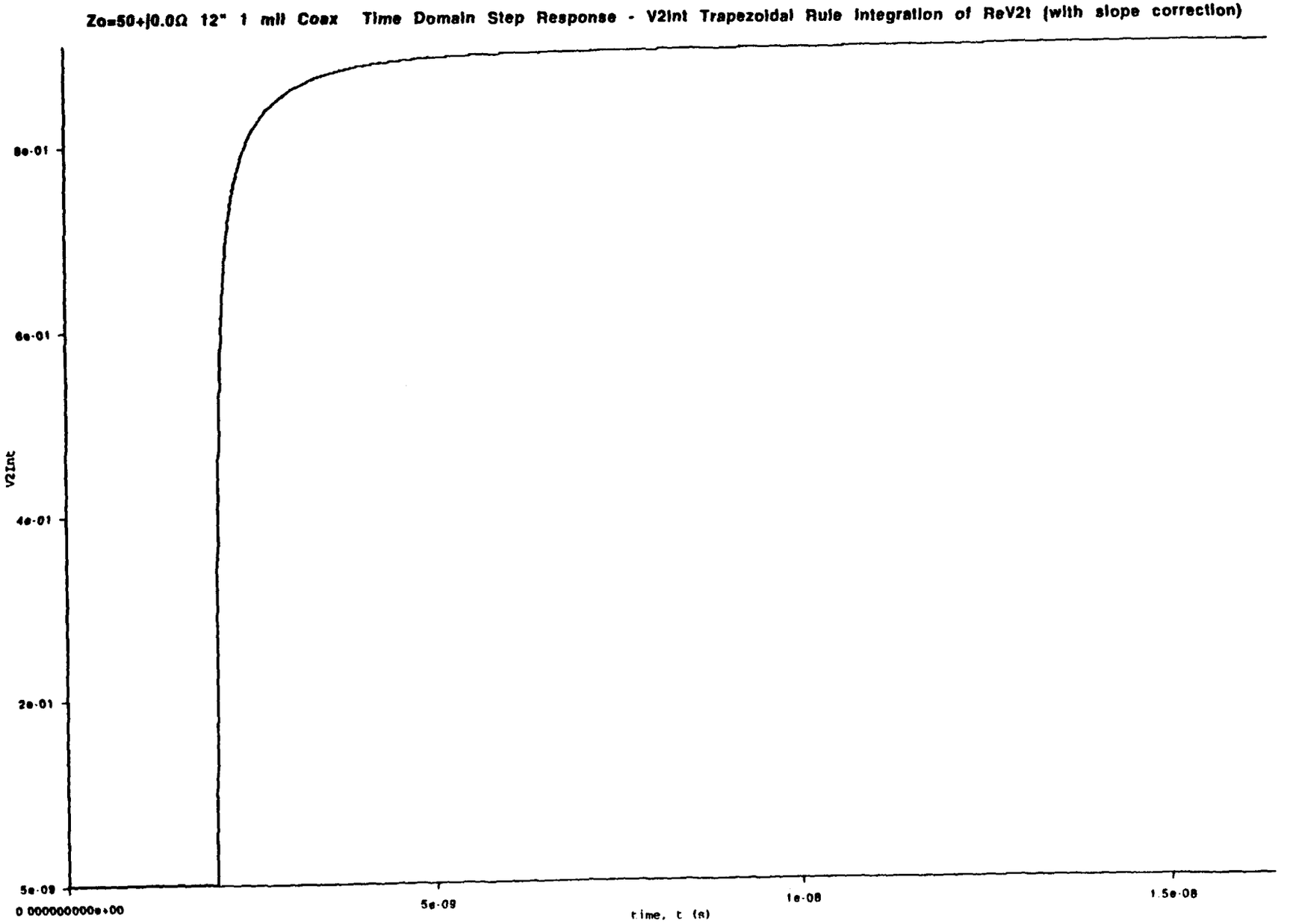

Zo=50+j0.0Ω 12" 1 mil Coax Time Domain Step Response - V2int Trapezoidal Rule Integration of ReV2t (with slope correction)
8e-01
6e-01
4e-01
2e-01
5e-09
V2Int
0.000000000e+00
5e-09
1e-08
1.5e-08
time, t (s)

Figure 32

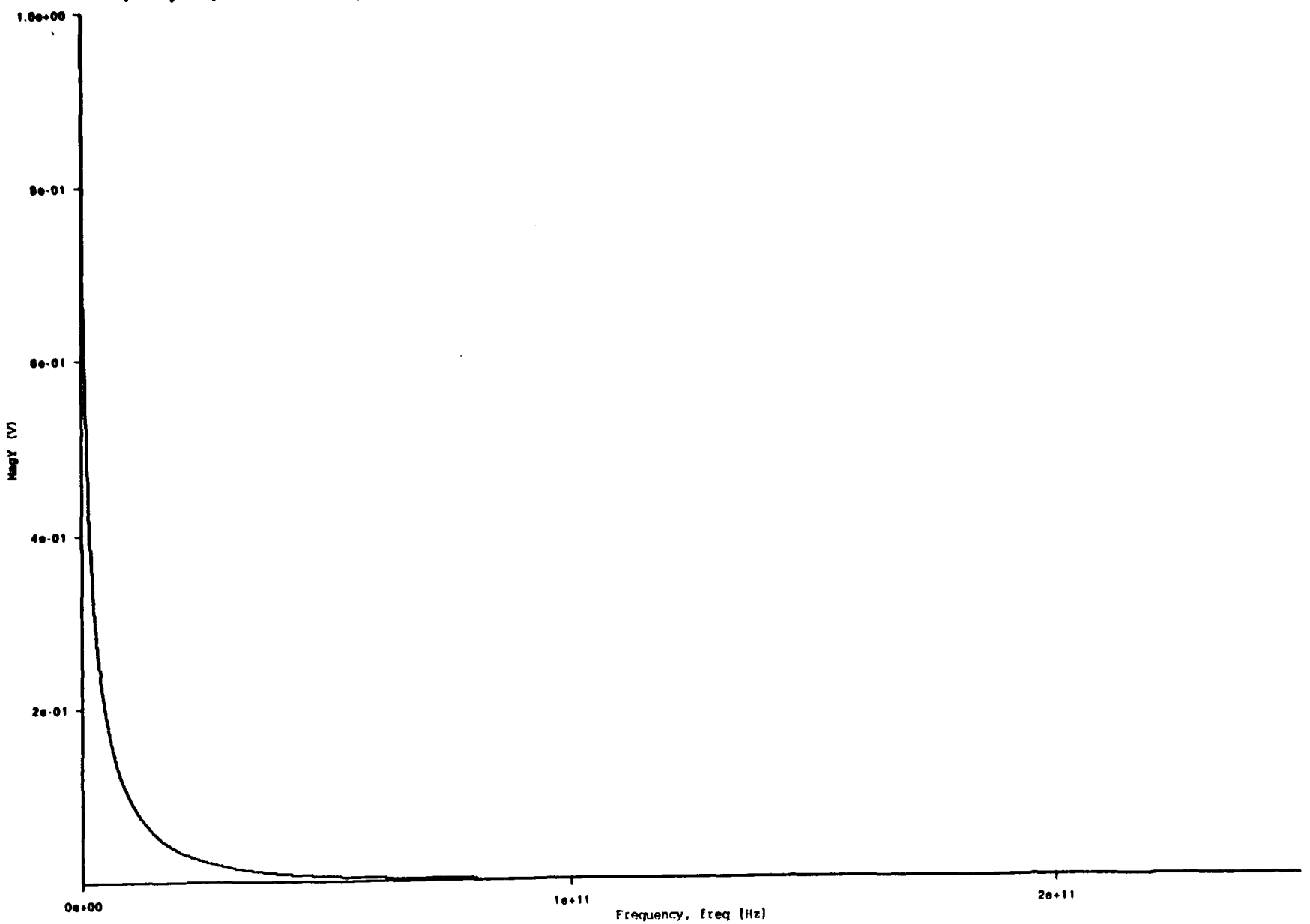

Frequency Dependence of Magnitude of Open-Circuit Voltage at end of 12" of 1/2 mil Cu Coax Line (Ber/Bel Calc. of Rac and Lint)
1.0e+00
8e-01
6e-01
4e-01
2e-01
MagY (V)
0e+00
1e+11
2e+11
Frequency, freq (Hz)

Figure 33

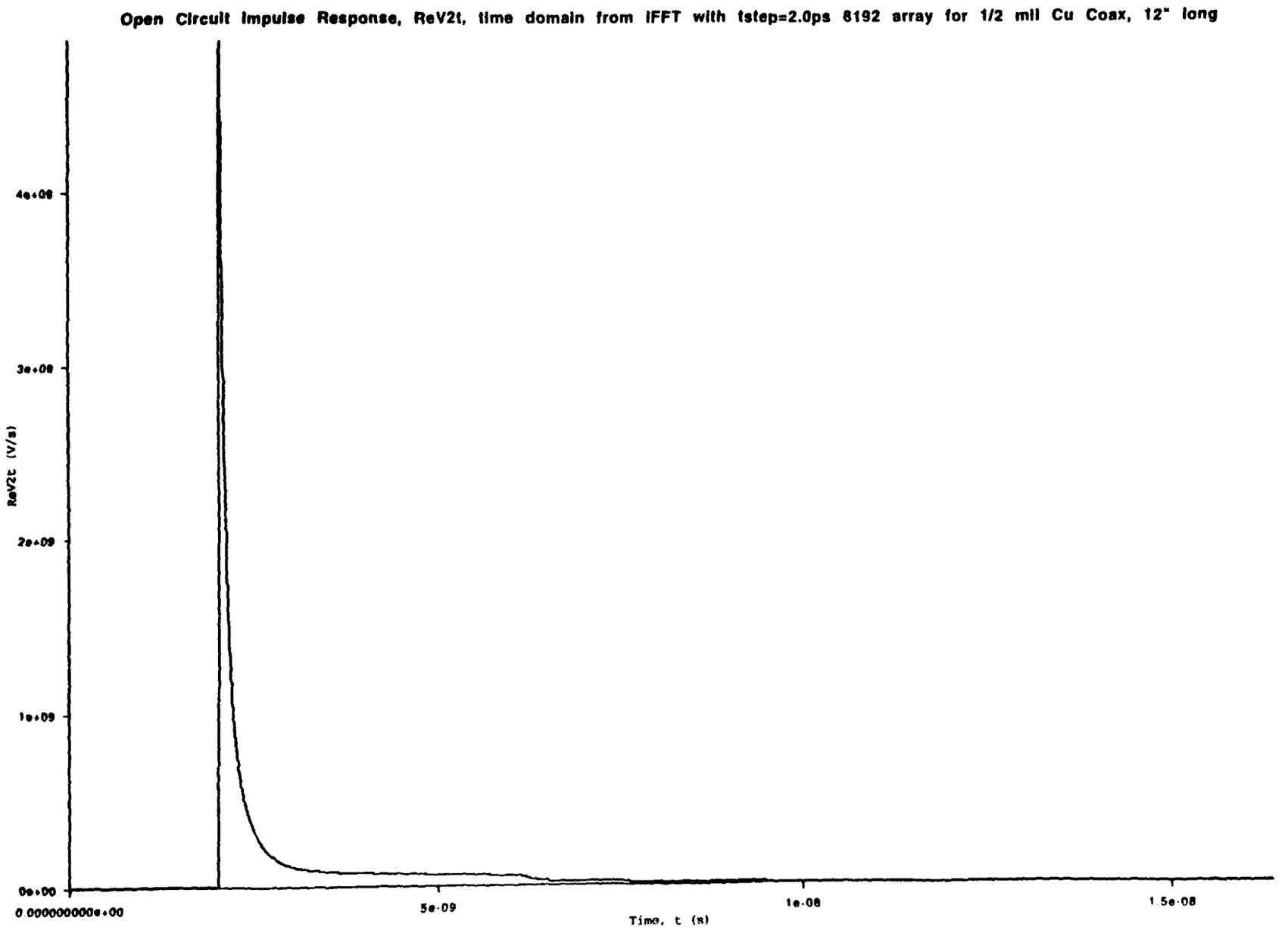

Open Circuit Impulse Response, ReV2t, time domain from IFFT with tstep=2.0ps 8192 array for 1/2 mil Cu Coax, 12" long
4e+09
3e+09
2e+09
1e+09
0e+00
ReV2t (V/s)
0.000000000e+00
5e-09
1e-08
1.5e-08
Time, t (s)

Figure 34

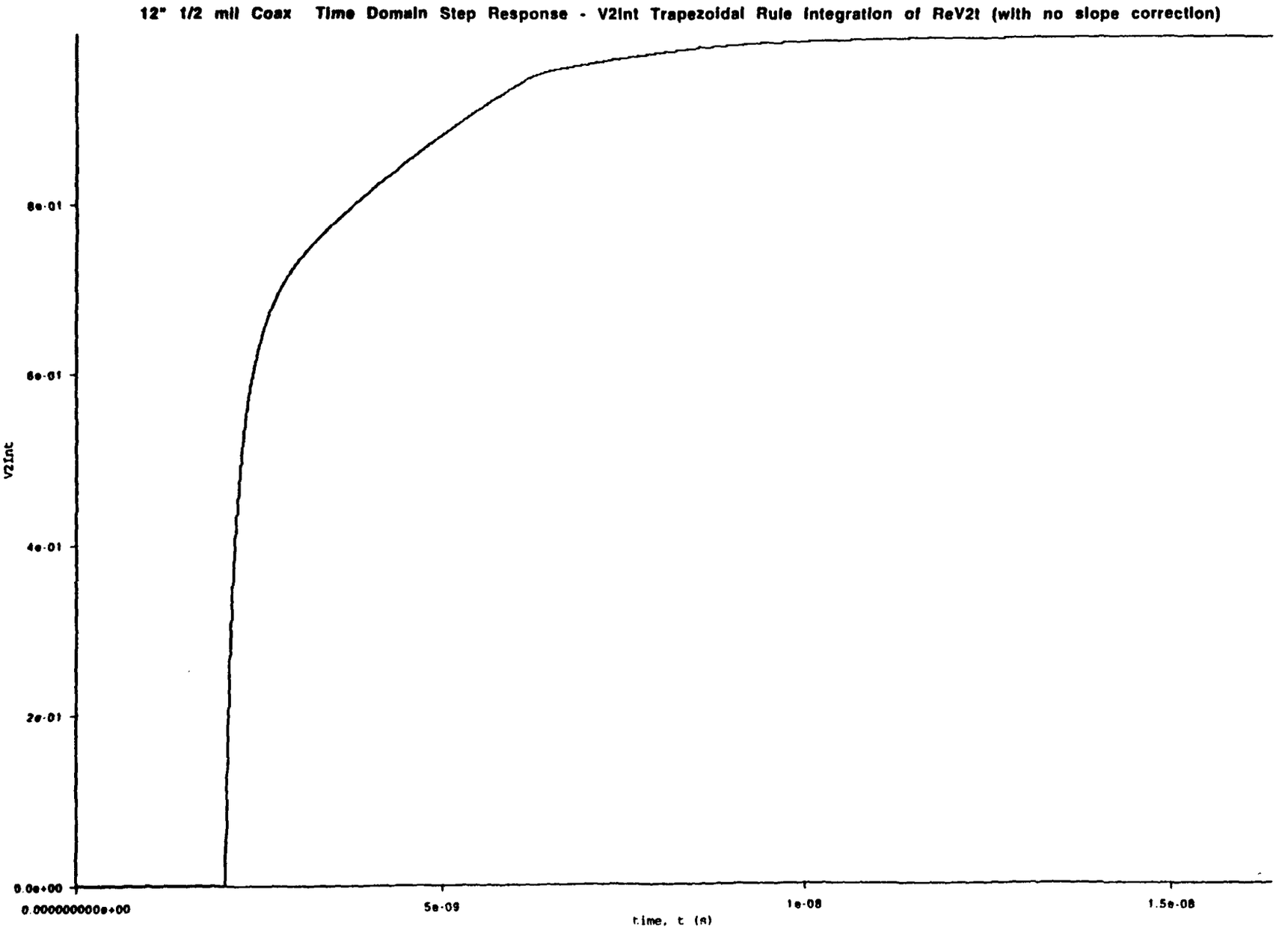

12" 1/2 mil Coax Time Domain Step Response - V2int Trapezoidal Rule Integration of ReV2t (with no slope correction)
V2int
8e-01
6e-01
4e-01
2e-01
0.0e+00
0.000000000e+00
5e-09
1e-08
1.5e-08
time, t (s)

Figure 35

Section 2.0

Commercialization of High Temperature Superconducting Technology

2.1. Background

For the quarter ending June 1992 much of the emphasis was directed at working out a cryoelectronic plan that could be sold to DARPA management and one that would culminate in an industry driven by this technology. It is now accepted that while the high end system market may be the first to start designing into cryoelectronic, the stable part of the industry has got to come from the high part of the low end such as the workstation. That is where the volume market will be and that is where we think we can make a significant impact.

When we began this project we were thinking of it as a long term program waiting for breakthroughs in HTSC materials and MCM processes. This approach has now been expanded significantly. We have recommended to DARPA that HTSC-MCM should be considered as part of a bigger cryoelectronic technology which goes beyond 77°K operation and start thinking about a cascaded approach which begins at around 200°K and works its way down to 77°K. In view of the fact that future IC foundries will be very costly, in excess of $1B per foundry, and in view of the fact that larger IC's may not have the performance that has been anticipated, it may be that low temperature IC operations could bring in a much more favorable price-performance characteristic in a very near short time using a modified and optimized IC process directed for low temperature operations. To our pleasant surprise we find the same type of thinking in industry be it high end or low end computer systems.

During the last few months a number of meetings were held at SUN, STI, Carrier, Cray, E-Systems, Datamax and DEC. All of these companies now seem to be converging towards a cryoelectronic technology thrust that can meet our business criteria close to an affordable budget.

The bottom line is this: a merchant cryoelectronic infrastructure led by a company such as STI needs to be developed to service the systems industry. This company would want to supply cryo-subassembiles to system houses. They would work IC foundries to optimize IC for cryoelectronics and set up the mechanics to market them to the industry. They would work with the CAD tools industry to ensure a complete suite for the cryoelectronic industry is available and that equipment for packaging and testing the ICs can be developed. Most importantly they would work to see that a cost effective highly reliable cryogenics be available within two years.

Extensive discussions of this approach took place with SUN, Cray, and DEC. Programs with these companies are proprietary and cannot be discussed in this report. However, based on these discussions, a four year cryoelectronics plan was developed and submitted to F. Patten at DARPA. In this plan, details were given about the requirements for infrastructure technology elements development, applications both commercial and military, required budgets, milestones, and timelines. This report can be accessed through Dr. Patten.